NEC

TFT COLOR LCD MODULE

NL3224BC35-20

13.9cm (5.5 Type)
QVGA

DATA SHEET

(3rd edition)

All information is subject to change without notice.

Document Number: EN0556EJ3V0DS00 (3rd edition)
Published date: March 2002 N CP(N)

INTRODUCTION

While NEC Corporation has been making continuous effort to enhance the reliability of its products, the possibility of failures cannot be eliminated entirely. To minimize risks of damage to property or injury to person arising from a failure in an NEC product, customers must incorporate sufficient safety measures in their design, such as redundancy, fire-containment and anti-failure features.

NEC products are classified into the following three quality grades:

"Standard", "Special", "Specific"

The ***"Specific"*** quality grade applies only to applications developed based on a customer designated "quality assurance program" for a specific application. The recommended applications of a product depend on its quality grade, as indicated below. Customers must check the quality grade of each application before using it in a particular application.

Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots

Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)

Specific: Military systems, aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems (medical equipment, etc.) and any other equipment

The quality grade of this product is ***"Standard"*** unless otherwise specified in this document. If customers intend to use this product for applications other than those specified for ***"Standard"*** quality grade, they should contact NEC Corporation sales representative in advance.

Anti-radioactive design is not implemented in this product.

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1. OUTLINE

1.1 STRUCTURE AND PRINCIPLE

NL3224BC35-20 module is composed of the amorphous silicon thin film transistor liquid crystal display (a-Si TFT LCD) panel structure with driver LSIs for driving the TFT (Thin Film Transistor) array and a backlight unit.

The a-Si TFT LCD panel structure is injected liquid crystal material into a narrow gap between the TFT array glass substrate and a color-filter glass substrate.

Color (Red, Green, Blue) data signals from a host system (e.g. PC, signal generator, etc.) are modulated into best form for active matrix system by a signal processing board, and sent to the driver LSIs which drive the individual TFT arrays.

The TFT array as an electro-optical switch regulates the amount of transmitted light from the backlight assembly, when it is controlled by data signals. Color images are created by regulating the amount of transmitted light through the TFT array of red, green and blue dots.

1.2 APPLICATIONS

- Industrial PC
- Display terminal for control system
- POS (Point of sale) terminal

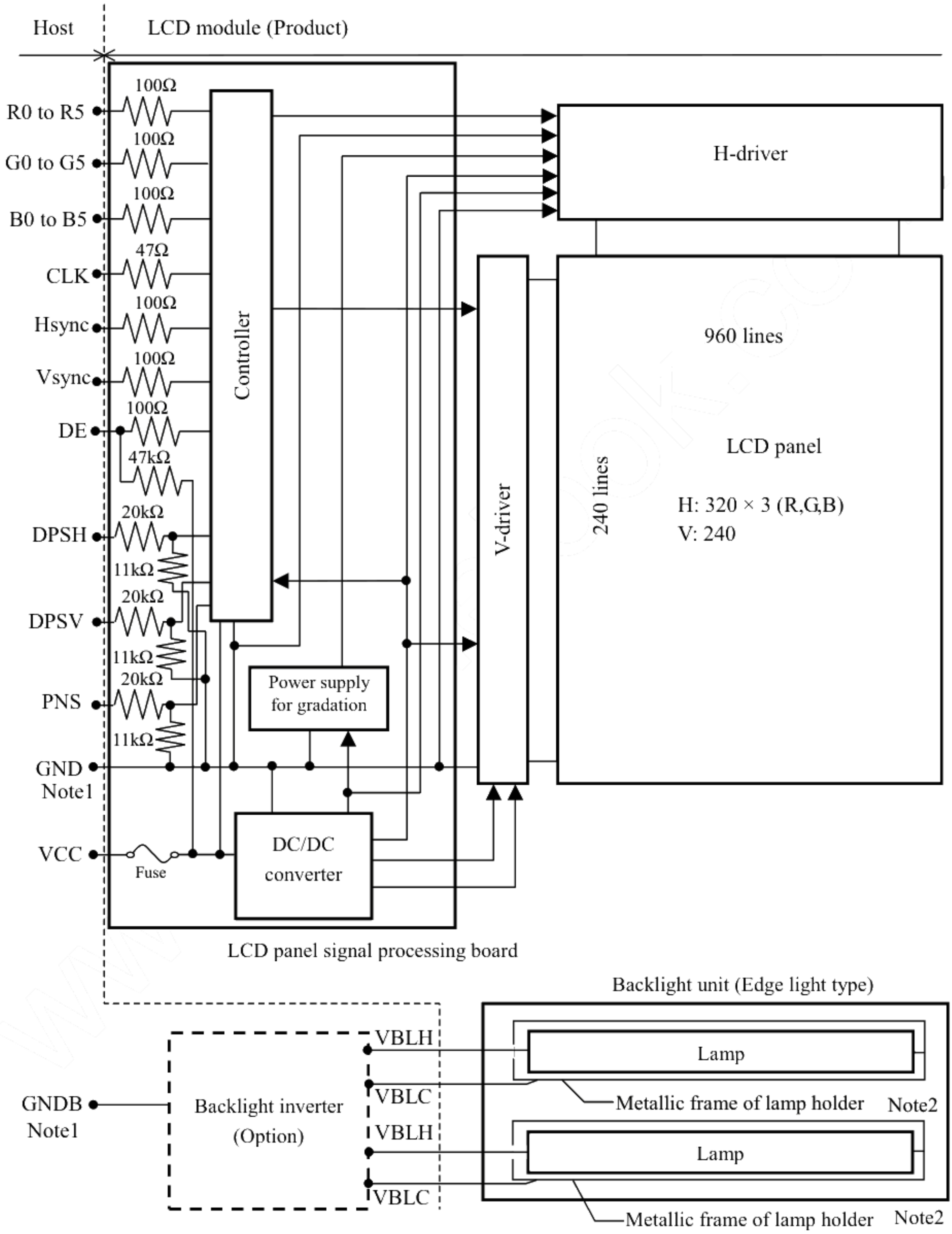
1.3 FEATURES

- High luminance
- Wide color gamut
- Wide viewing angle
- Low reflection
- 6-bit digital RGB signals
- Reversible-scan direction
- Edge light type
- Replaceable lamp for backlight unit (Inverter less)
- Acquisition product for UL/c-UL (File number: E170632)

2. GENERAL SPECIFICATIONS

Display area	111.4 (W) × 83.5 (H) mm
Diagonal size of display	13.9 cm (5.5 inches)
Drive system	a-Si TFT active matrix
Display color	262,144 colors
Pixel	*At QVGA display mode* 320 (H) × 240 (V) pixels *At VGA display mode* 640 (H) × 480 (V) pixels (Display area: 320 (H) × 240 (V) pixels)
Pixel arrangement	RGB (Red dot, Green dot, Blue dot) vertical stripe
Dot pitch	0.1160 (W) × 0.3480 (H) mm
Pixel pitch	0.3480 (W) × 0.3480 (H) mm
Module size	134.0 (W) × 104.5 (H) × 12.5 (D) mm (typ.)
Weight	210 g (typ.)
Contrast ratio	400:1 (typ.)
Viewing angle	*At the contrast ratio 10:1* • Horizontal: Left side 65° (typ.), Right side 65° (typ.) • Vertical: Up side 40° (typ.), Down side 65° (typ.)
Designed viewing direction	*At DPSH: normal scan and DPSV: normal scan* • Viewing direction without image reversal: up side (12 o'clock) • Viewing direction with contrast peak: down side 5° to 10° (6 o'clock) • Viewing angle with optimum grayscale (γ=2.2): normal axis
Polarizer surface	Antiglare treatment
Polarizer pencil-hardness	3H (min.) [by JIS K5400]
Color gamut	*At LCD panel center* 50 % (typ.) [against NTSC color space]
Response time	5 ms (typ.)
Luminance	*At 5.0mArms / lamp* 400 cd/m^2 (typ.)
Signal system	6-bit digital signals for data of RGB colors, Dot clock (CLK), Data enable (DE), Horizontal synchronous signal (Hsync), Vertical synchronous signal (Vsync)
Power supply voltage	LCD panel signal processing board: 3.3V or 5.0V
Backlight	Edge light type: 2 cold cathode fluorescent lamps (Replaceable parts • Lamps for backlight unit: Type No. 55LHS11) (Recommended inverter (Option) • Inverter: Type No. 55PW131)
Power consumption	*At maximum luminance and checkered flag pattern* 4.1 W (typ.)

3. BLOCK DIAGRAM



Note1: GND and GNDB (Backlight inverter ground) should be connected together in customer equipment.
Note2: The metallic frame of lamp holder is used to a transmission line for VBLC.

4. DETAILED SPECIFICATIONS

4.1 MECHANICAL SPECIFICATIONS

Parameter	Specification		Unit
Module size	134.0 ± 0.5 (W) × 104.5 ± 0.5 (H) × 12.5 ± 0.5 (D)	Note1	mm
Display area	111.4 (W) × 83.5 (H)	Note1	mm
Weight	215 (typ.), 220 (max.)		g

Note1: See "**7. OUTLINE DRAWINGS**".

4.2 ABSOLUTE MAXIMUM RATINGS

Parameter			Symbol	Rating	Unit	Remarks
Power supply voltage	LCD panel signal board		VCC	-0.3 to +6.5	V	Ta = 25°C
	Lamp	High voltage side (Hot) Note1	VBLH	1,500	Vrms	
		Low voltage side (Cold) Note2	VBLC	42.4	Vrms	
Input voltage for signals	Display signals Note3		VD	-0.3 to VCC+0.3	V	
	Function signals Note4		VF	-0.3 to VCC+0.3	V	
Storage temperature			Tst	-30 to +80	°C	-
Operating temperature	Front surface		TopF	-10 to +70	°C	
	Rear surface		TopR	-10 to +75	°C	
Relative humidity Note5			RH	≤ 95	%	Ta ≤ 40°C
				≤ 85	%	40 < Ta ≤ 50°C
				≤ 70	%	50 < Ta ≤ 55°C
				≤ 60	%	55 < Ta ≤ 60°C
				≤ 50	%	60 < Ta ≤ 65°C
				≤ 42	%	65 < Ta ≤ 70°C
Absolute humidity Note5			AH	≤ 78 Note6	g/m^3	Ta > 70°C

Note1: "VBLH" is the voltage value between low voltage terminal (Cold) and high voltage terminal (Hot).

Note2: "VBLC" is the voltage value between backlight inverter ground (GNDB) and low voltage terminal (Cold).

Note3: Display signals are CLK, Hsync, Vsync, DE and DATA (R0 to R5, G0 to G5, B0 to B5).

Note4: Function signals are DPSH, DPSV and PNS.

Note5: No condensation

Note6: Ta = 70°C, RH = 42%

4.3 ELECTRICAL CHARACTERISTICS

4.3.1 Driving for LCD panel signal processing board

(Ta = 25°C)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Remarks
Power supply voltage		VCC	3.0	3.3	3.6	V	for 3V system
			4.75	5.00	5.25	V	for 5V system
Power supply current		ICC	-	180 Note1	250	mA	VCC = 3.3V Note2
			-	120 Note1	165	mA	VCC = 5.0V Note2
Logic input voltage for display signals	Low	VDLL	0	-	0.3Vcc	V	CMOS level
	High	VDLH	0.7Vcc	-	Vcc	V	
Input voltage for DPSH or DPSV signals	Low	VFDL	0	-	0.3Vcc	V	
	High	VFDH	0.7Vcc	-	Vcc	V	
Input voltage for PNS signal	Low	VFPL	0	-	0.3Vcc	V	
	High	VFPH	0.7Vcc	-	Vcc	V	

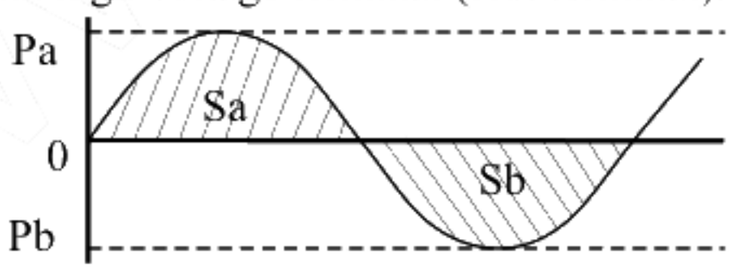
Note1: Checkered flag pattern [by EIAJ ED-2522]
Note2: At QVGA display mode (PNS: Low)

4.3.2 Working for backlight lamp

Parameter	Symbol	Ta	Min.	Typ.	Max.	Unit	Remarks
Starting voltage	VS	-10°C	780	-	-	Vrms	Note1
		25°C	550	-	-	Vrms	
Power supply voltage	VBLH	25°C	-	350	-	Vrms	Note1,Note2
Power supply current	IBL	25°C	4.5	5.0	5.5	mArms	Note2
Oscillation frequency	FO	25°C	39	43	47	kHz	Note3

Note1: The power supply voltage cycle between lamps should be kept on a same phase. "VS" and "VBLH" are the voltage value between low voltage side (Cold) and high voltage side (Hot).

Note2: The asymmetric ratio of working waveform for lamps (Power supply voltage peak ratio, power supply current peak ratio and waveform space ratio) should be less than 5 % (See the following figure.). If the waveform is asymmetric, DC (Direct current) element apply into the lamp. In this case, a lamp lifetime may be shortened, because a distribution of a lamp enclosure substance inclines toward one side between low voltage terminal (Cold terminal) and high voltage terminal (Hot terminal).



$$\frac{|Pa - Pb|}{Pb} \times 100 \leq 5\ \%$$

$$\frac{|Sa - Sb|}{Sb} \times 100 \leq 5\ \%$$

Pa: Supply voltage/current peak for positive, Pb: Supply voltage/current peak for negative
Sa: Waveform space for positive part, Sb: Waveform space for negative part

Note3: In case "FO" is not the recommended value, beat noise may display on the screen, because of interference between "FO" and "1/th". Recommended value of "FO" is as following.

$$FO = \frac{1}{4} \times \frac{1}{th} \times (2n\text{-}1)$$

th: Horizontal synchronous cycle (See "4.9.7 Timing characteristics for QVGA display mode" or "4.9.8 Timing characteristics for VGA display mode".)

n: Natural number (1, 2, 3 ·····)

4.3.3 Power supply voltage ripple

This product works, even if the ripple voltage levels are beyond the permissible values as following the table, but there might be noise on the display image.

Parameter	Power supply voltage	Ripple voltage Note1 (Measure at input terminal of power supply)	Unit
VCC	3.3 V	≤ 100	mVp-p
	5.0 V	≤ 100	mVp-p

Note1: The permissible ripple voltage includes spike noise.

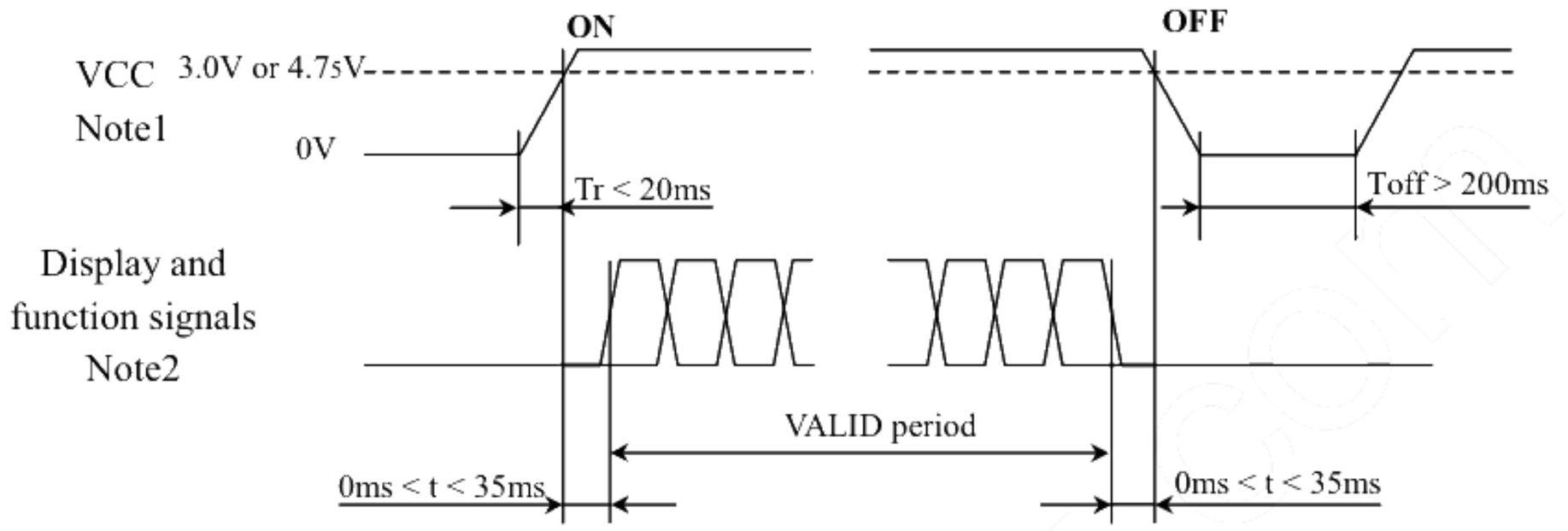
4.3.4 Fuse

Fusing line	Fuse		Rating	Fusing current Note1
	Type	Supplier		
VCC	ICP-S1.8	ROHM Co., Ltd.	1.8 A 50 V	4.0 A

Note1: The power supply capacity should be more than the fusing current. If the power supply capacity is less than the fusing current, the fuse may not blow for a short time, and then nasty smell, smoking and so on may occur.

4.4 POWER SUPPLY VOLTAGE SEQUENCE

4.4.1 Sequence for LCD panel signal processing board

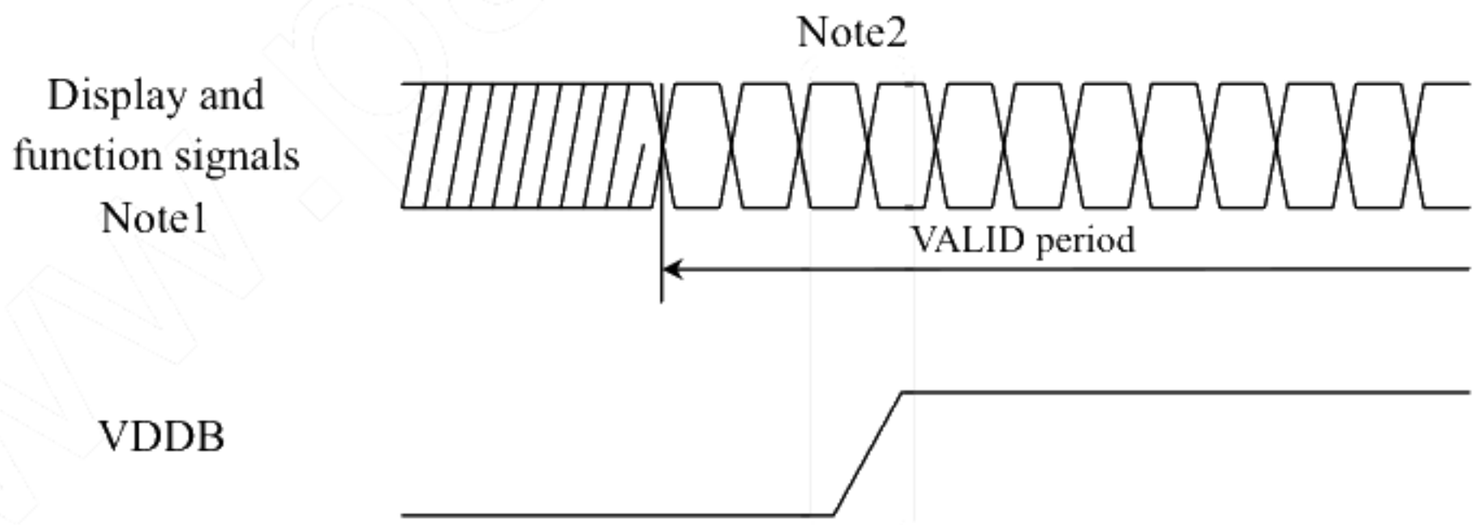


Note1: In terms of voltage variation (voltage drop) while VCC rising edge is below 3.0V in "VCC = 3.3V" or 4.75V in "VCC = 5.0V", a protection circuit may work, and then this product may not work.

Note2: Display (CLK, Hsync, Vsync, DE, R0 to R5, G0 to G5, B0 to B5) and function (DPSH, DPSV, PNS) signals must be Low or High-impedance, exclude the VALID period (See above sequence diagram), in order to avoid that internal circuits is damaged.

If some of display and function signals of this product are cut while this product is working, even if the signal input to it once again, it might not work normally. If customer stops the display and function signals, they should be cut VCC.

4.4.2 Sequence for backlight inverter (Option)



Note1: These are display and function signals for LCD panel signal processing board.

Note2: The backlight inverter voltage (VDDB) should be inputted within the valid period of display and function signals, in order to avoid unstable data display.

4.5 CONNECTIONS AND FUNCTIONS FOR INTERFACE PINS

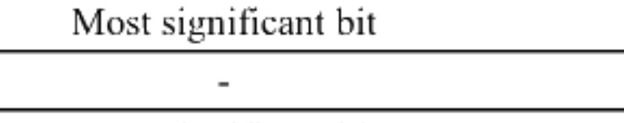
4.5.1 LCD panel signal processing board

CN1 socket (LCD module side): 08-6210-033-340-800 (Kyocera Elco Corp.)
Adaptable plug: TW-VF-33-0.035 TA-200-A4.0BB-P0.5-HBL8 (Fujikura Ltd.)

Pin No.	Symbol	Signal	Remarks
1	GND	Ground	-
2	CLK	Dot clock	
3	Hsync	Horizontal synchronous	
4	Vsync	Vertical synchronous	
5	GND	Ground	
6	R0	Red data (LSB)	Least significant bit
7	R1	Red data	-
8	R2	Red data	
9	R3	Red data	
10	R4	Red data	
11	R5	Red data (MSB)	Most significant bit
12	GND	Ground	-
13	G0	Green data (LSB)	Least significant bit
14	G1	Green data	-
15	G2	Green data	
16	G3	Green data	
17	G4	Green data	
18	G5	Green data (MSB)	Most significant bit
19	GND	Ground	-
20	B0	Blue data (LSB)	Least significant bit
21	B1	Blue data	-
22	B2	Blue data	
23	B3	Blue data	
24	B4	Blue data	
25	B5	Blue data (MSB)	Most significant bit
26	GND	Ground	-
27	DE	Select of DE / Fixed mode	DE mode: Data enable signal, Fixed mode: Open
28	VCC	Power supply	-
29	VCC	Power supply	
30	DPSH	Select of scan direction (Horizontal)	Normal scan: Low or Open, Reverse scan: High Note1
31	DPSV	Select of scan direction (Vertical)	
32	PNS	Select of pixel number	QVGA mode: Low or Open, VGA mode: High Note1
33	GND	Ground	-

Note1: See "4.8 SCANNING DIRECTIONS".

CN1: Figure of socket

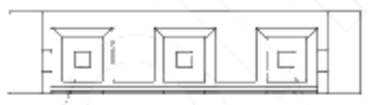


4.5.2 Backlight lamp

CN2 plug: BHR-03VS-1 (J.S.T Mfg. Co., Ltd.)
Adaptable socket: SM03 (4.0) B-BHS-TB (J.S.T Mfg. Co., Ltd.)

Pin No.	Symbol	Signal	Remarks
1	VBLH	High voltage (Hot)	Pink cable
2	NC	Non connection	-
3	VBLC	Low voltage (Cold)	White cable

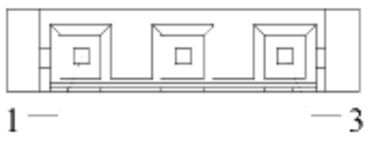
CN2: Figure of plug



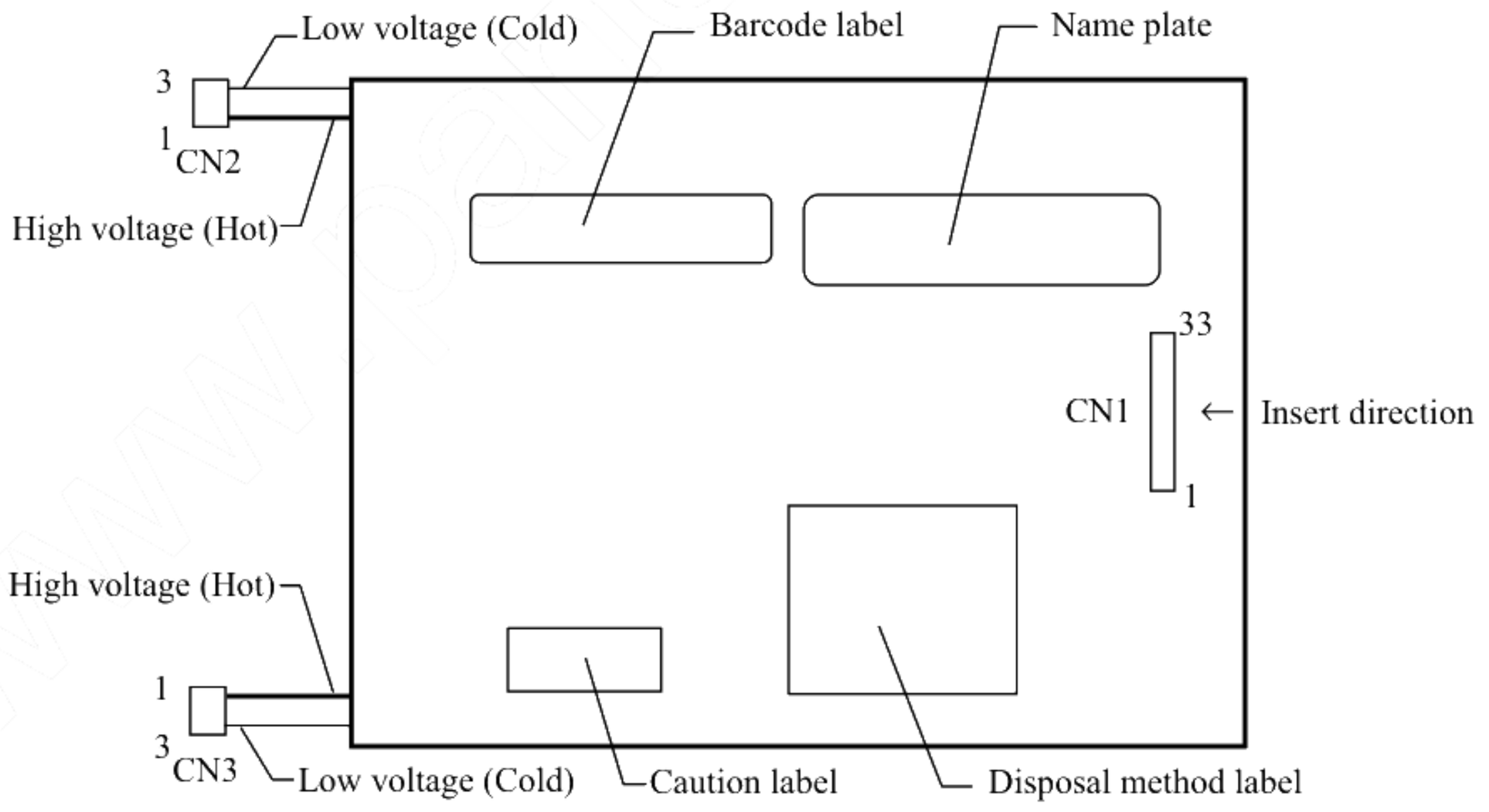
CN3 plug: BHR-03VS-1 (J.S.T Mfg. Co., Ltd.)
Adaptable socket: SM03 (4.0) B-BHS-TB (J.S.T Mfg. Co., Ltd.)

Pin No.	Symbol	Signal	Remarks
1	VBLH	High voltage (Hot)	Pink cable
2	NC	Non connection	-
3	VBLC	Low voltage (Cold)	White cable

CN3: Figure of plug



4.5.3 Positions of plugs and a socket



4.6 DISPLAY COLORS AND INPUT DATA SIGNALS

This product can display in equivalent to 262,144 colors in 64 scale. Also the relation between display colors and input data signals is as the following table.

Display colors		Data signal (0: Low level, 1: High level)																	
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Basic colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red scale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	dark	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	↑				:					:						:			
	↓				:					:						:			
	bright	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
		1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Green scale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	dark	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	↑				:					:						:			
	↓				:					:						:			
	bright	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0
		0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Blue scale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	↑				:					:						:			
	↓				:					:						:			
	bright	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1
		0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

4.7 DISPLAY POSITIONS

The following table is the coordinates per pixel (See figure of "4.8 SCANNING DIRECTIONS".).

C(0, 0)	C(1, 0)	•••	C(X, 0)	•••	C(318, 0)	C(319, 0)
C(0, 1)	C(1, 1)	•••	C(X, 1)	•••	C(318, 1)	C(319, 1)
⋮	⋮	⋮	⋮	⋮	⋮	⋮
C(0, Y)	C(1, Y)	•••	C(X, Y)	•••	C(318, Y)	C(319, Y)
⋮	⋮	⋮	⋮	⋮	⋮	⋮
C(0,238)	C(1,238)	•••	C(X,238)	•••	C(318,238)	C(319,238)
C(0,239)	C(1,239)	•••	C(X,239)	•••	C(318,239)	C(319,239)

4.8 SCANNING DIRECTIONS

4.8.1 QVGA display mode

The following figures are seen from a front view. Also the arrow shows the direction of scan.

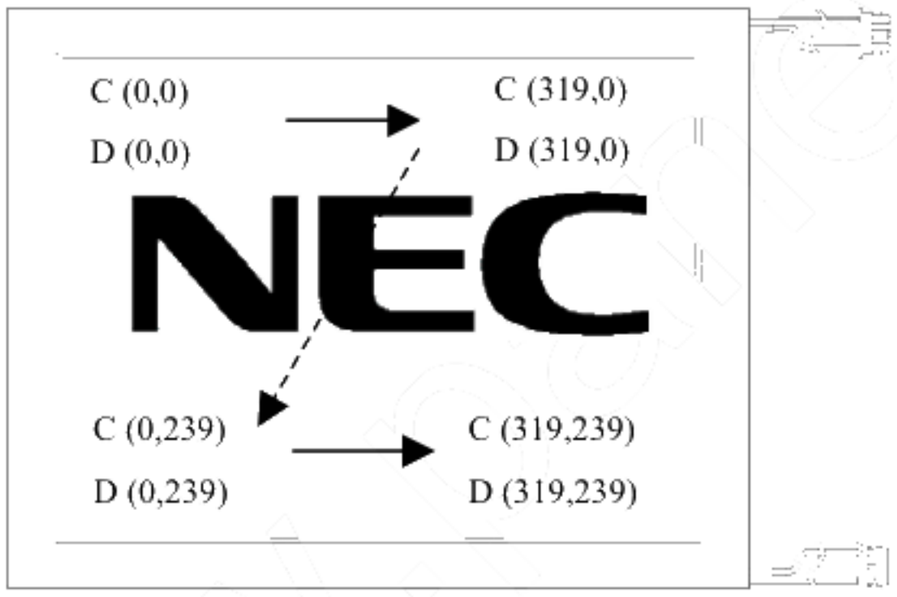


Figure 1. DPSH: Normal scan, DPSV: Normal scan

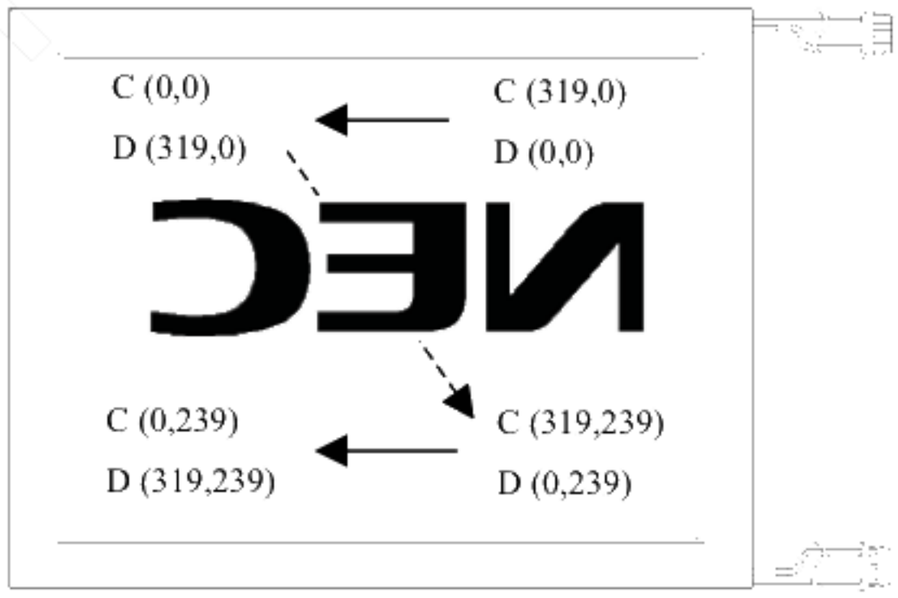


Figure 2. DPSH: Reverse scan, DPSV: Normal scan

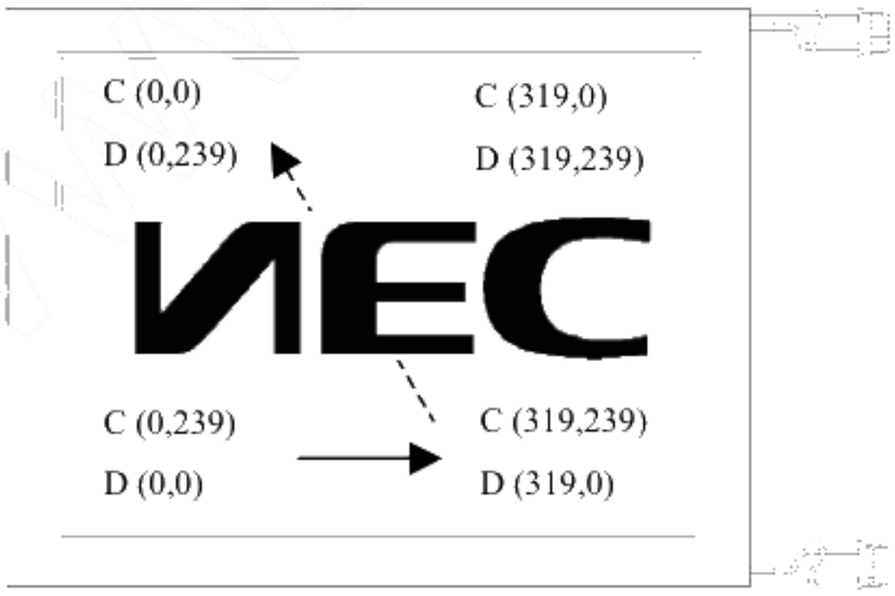


Figure 3. DPSH: Normal scan, DPSV: Reverse scan

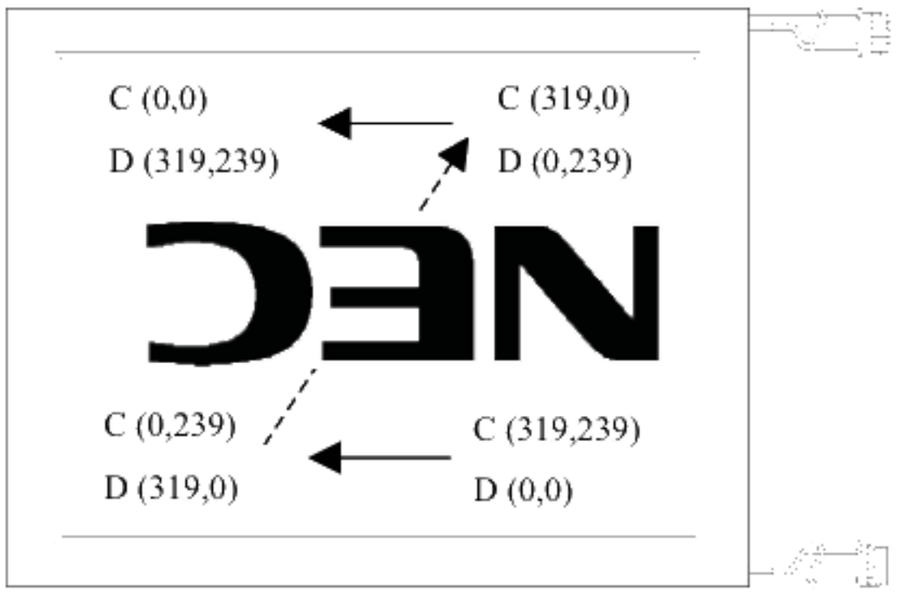


Figure 4. DPSH: Reverse scan, DPSV: Reverse scan

Note1: Meaning of C (X, Y) and D (X, Y)

C (X, Y): The coordinates of the display position (See "4.7 DISPLAY POSITIONS".)

D (X, Y): The data number of QVGA input signal for LCD panel signal processing board

Note2: Normal scan: Low or Open, Reverse scan: High

4.8.2 VGA display mode

The following figures are seen from a front view. Also the arrow shows the direction of scan, and a dotted line is a virtual display domain. In this display mode, only quarter domains of virtual display are displayed on the screen.

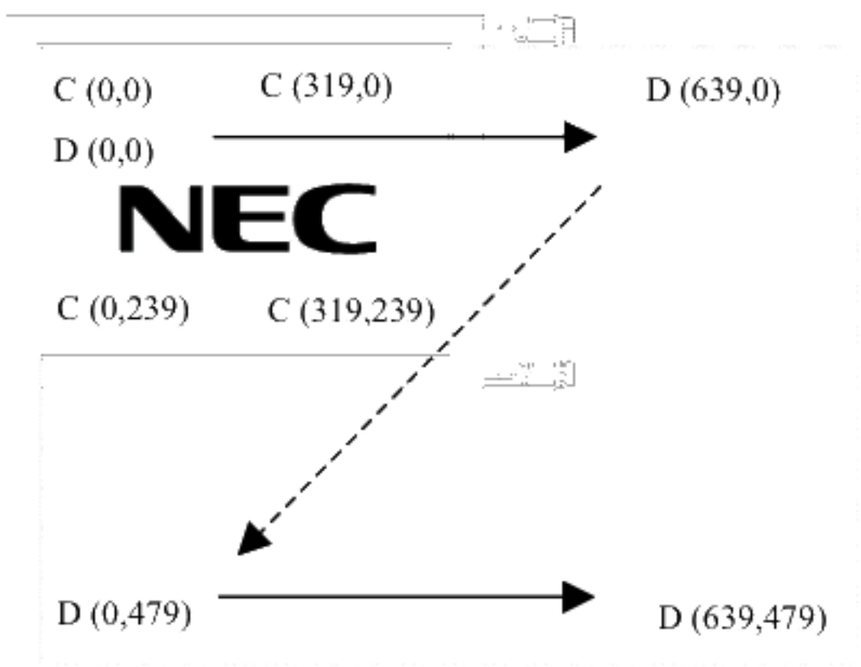


Figure 1. DPSH: Normal scan, DPSV: Normal scan

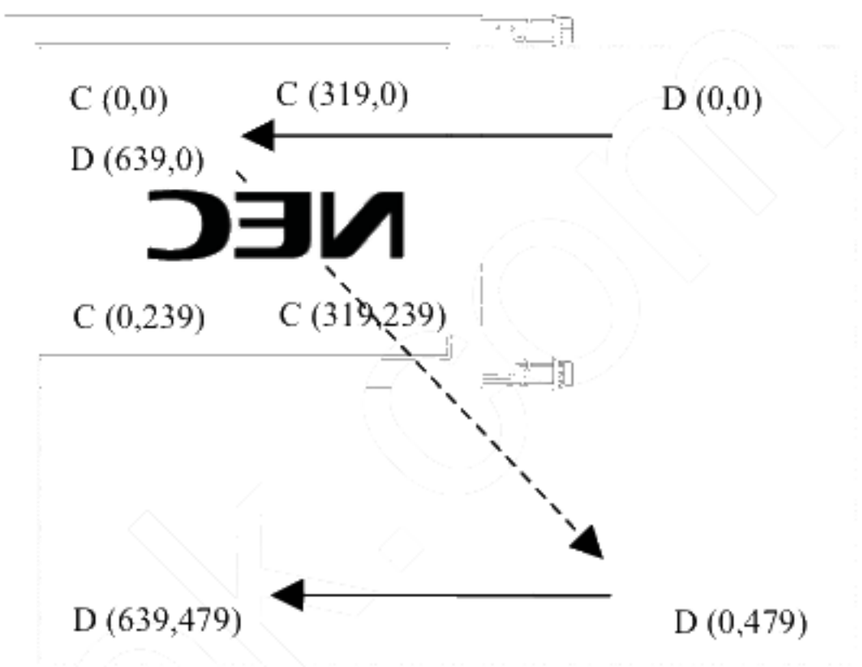


Figure 2. DPSH: Reverse scan, DPSV: Normal scan

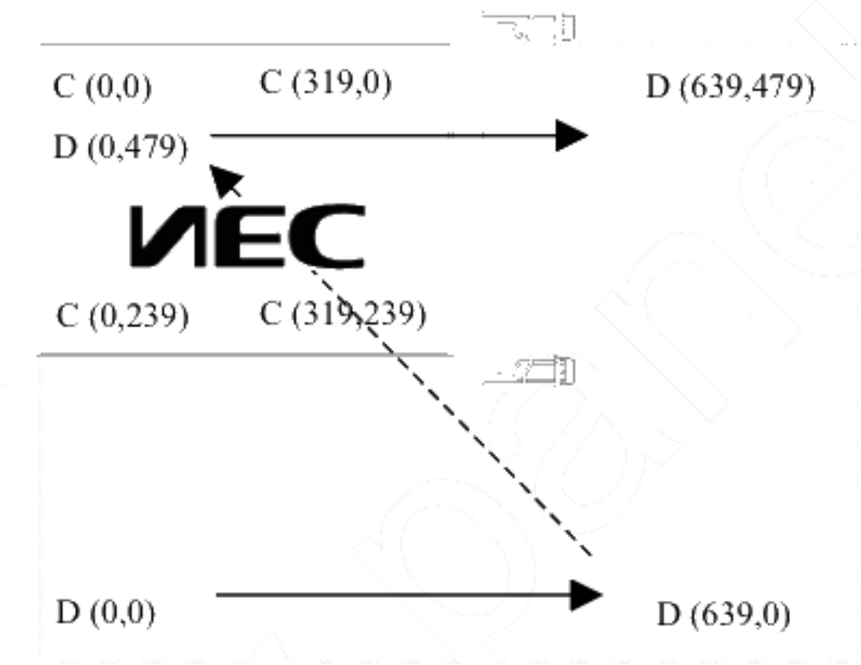


Figure 3. DPSH: Normal scan, DPSV: Reverse scan

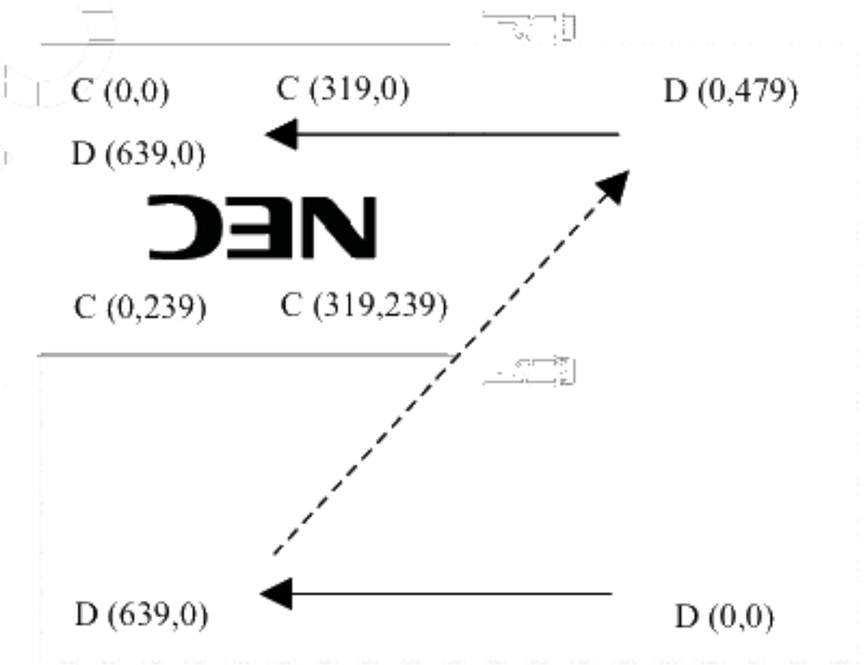


Figure 4. DPSH: Reverse scan, DPSV: Reverse scan

Note1: Meaning of C (X, Y) and D (X, Y)

C (X, Y): The coordinates of the display position (See "4.7 DISPLAY POSITIONS".)

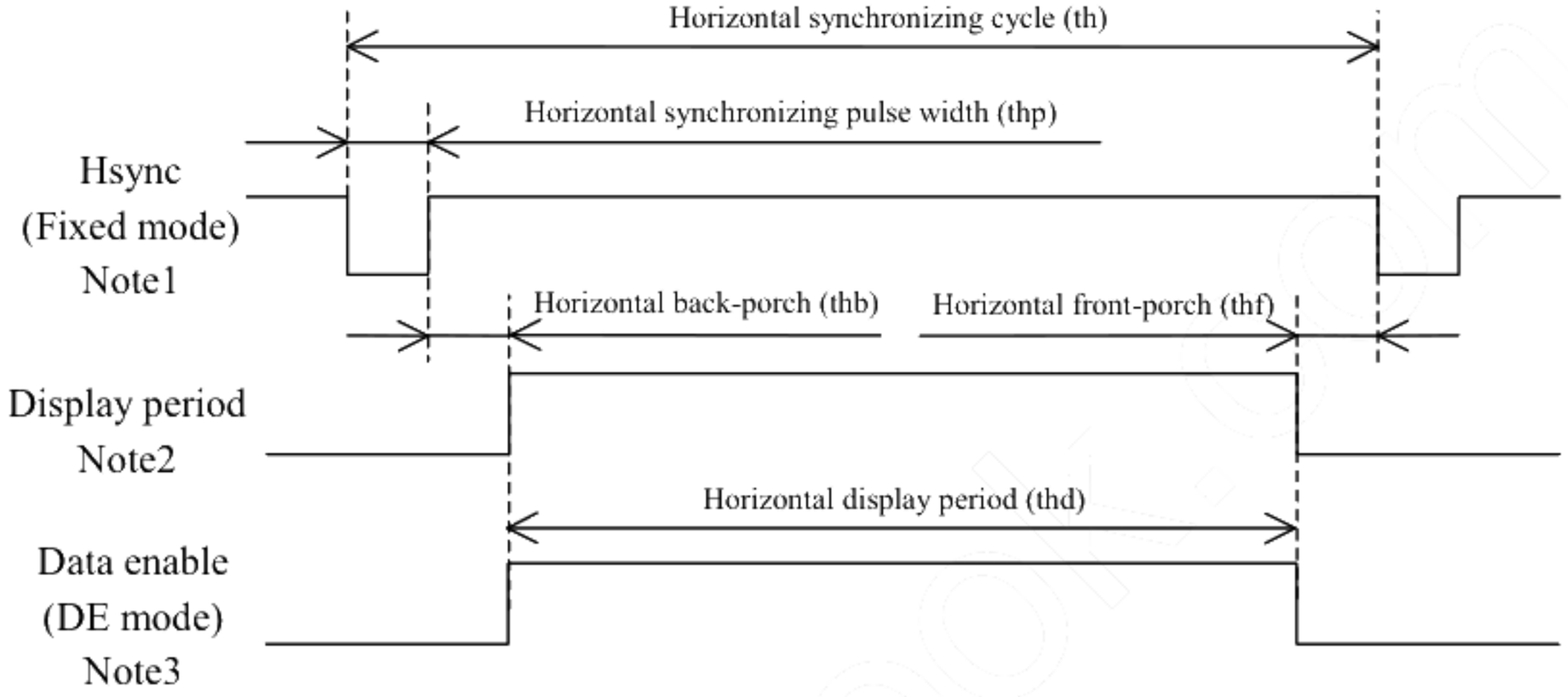
D (X, Y): The data number of VGA input signal for LCD panel signal processing board

Note2: Normal scan: Low or Open, Reverse scan: High

4.9 INPUT SIGNAL TIMINGS FOR LCD PANEL SIGNAL PROCESSING BOARD

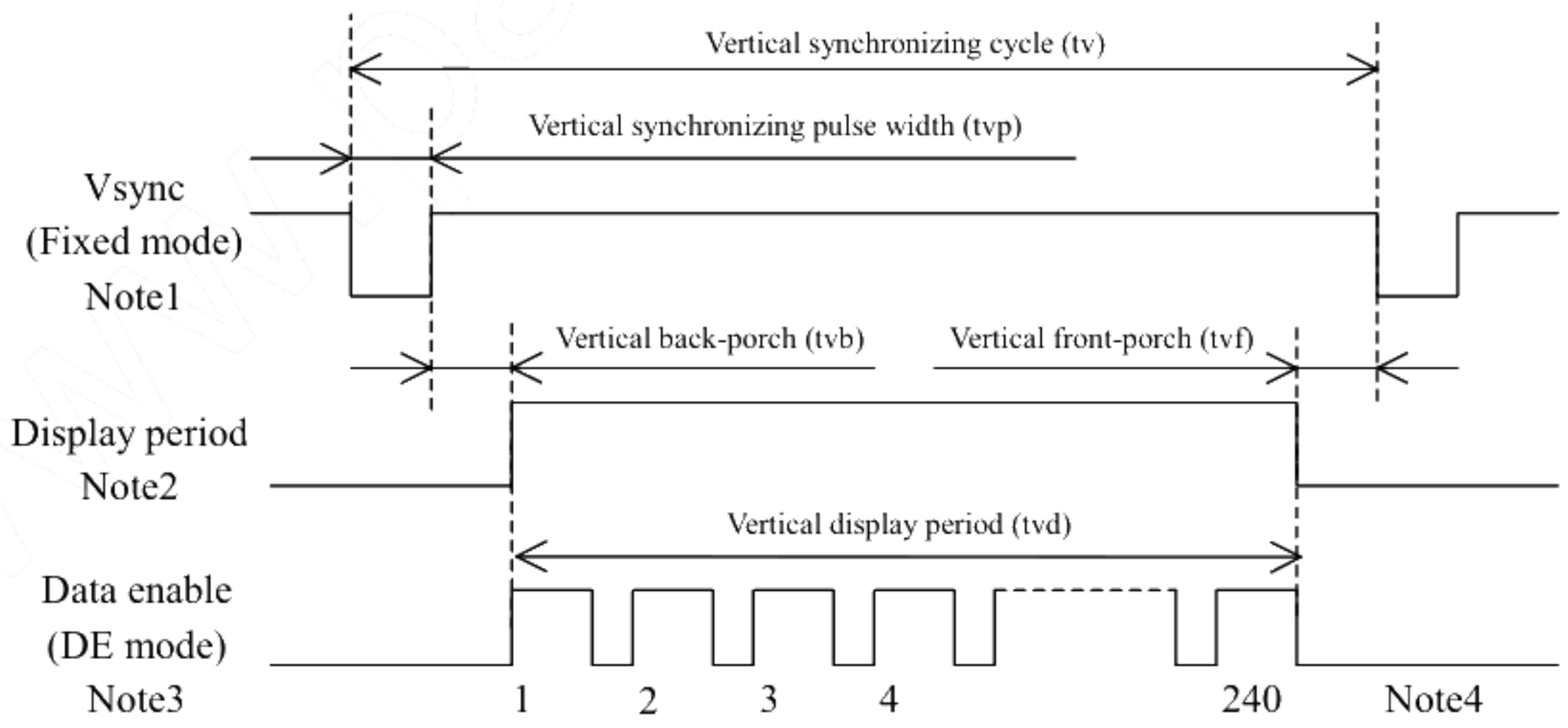
4.9.1 Outline of QVGA input signal timings

- Horizontal signal



Note1: Fixed mode cannot be used while working of DE mode.
Note2: This diagram indicates virtual signal for set up to timing.
Note3: Customer should be inputted synchronized signals (Hsync, Vsync) in addition to DE signal to this product, when it is worked in DE mode. Synchronized signals are used for DE/Fixed mode detection.

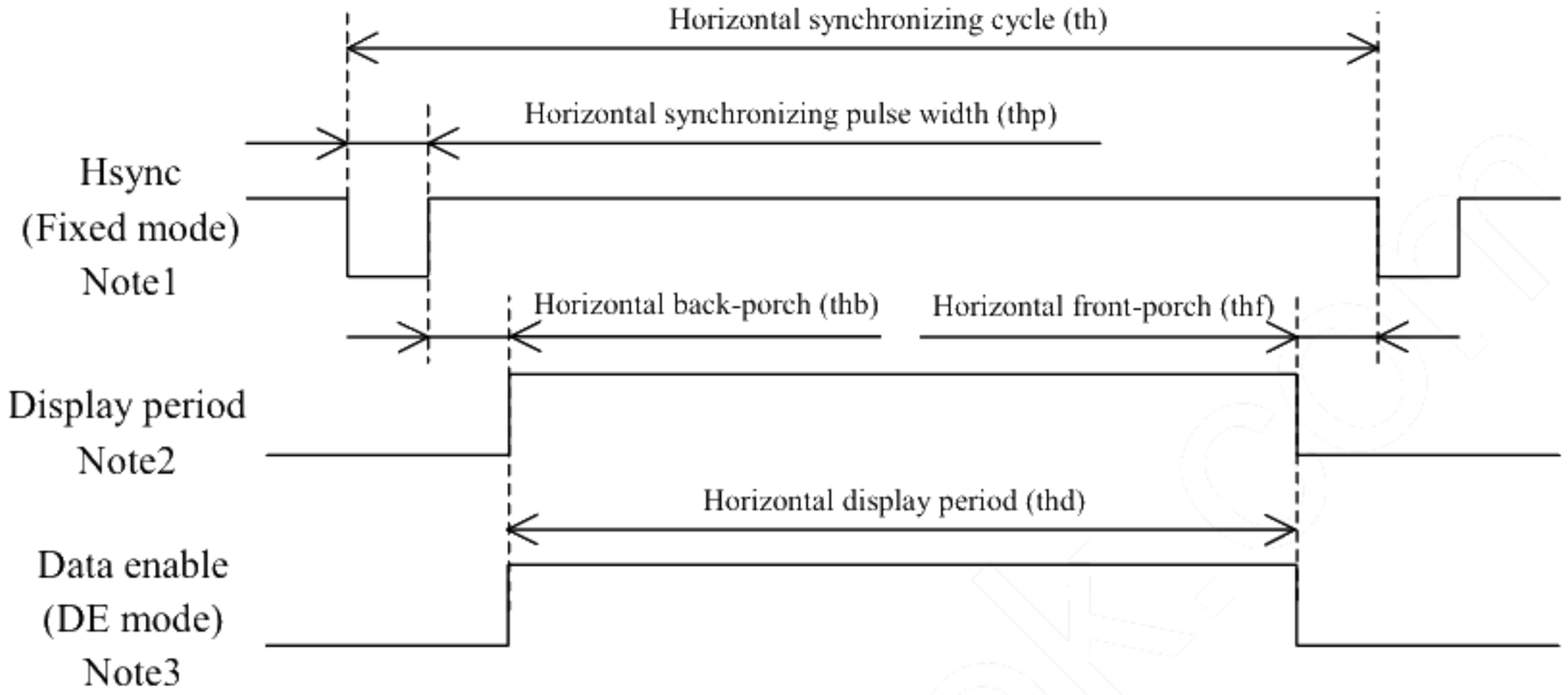
- Vertical signal



Note1: Fixed mode cannot be used while working of DE mode.
Note2: This diagram indicates virtual signal for set up to timing.
Note3: Customer should be inputted synchronized signals (Hsync, Vsync) in addition to DE signal to this product, when it is worked in DE mode. Synchronized signals are used for DE/Fixed mode detection.
Note4: See "4.9.3 Detailed QVGA input signal timing chart for fixed mode" and "4.9.4 Detailed QVGA input signal timing chart for DE mode" for numeration of pulse.

4.9.2 Outline of VGA input signal timings

• Horizontal signal



Note1: Fixed mode cannot be used while working of DE mode.

Note2: This diagram indicates virtual signal for set up to timing.

Note3: Customer should be inputted synchronized signals (Hsync, Vsync) in addition to DE signal to this product, when it is worked in DE mode. Synchronized signals are used for DE/Fixed mode detection.

• Vertical signal

Note3	1	2	3	4		480	Note4

Note1: Fixed mode cannot be used while working of DE mode.

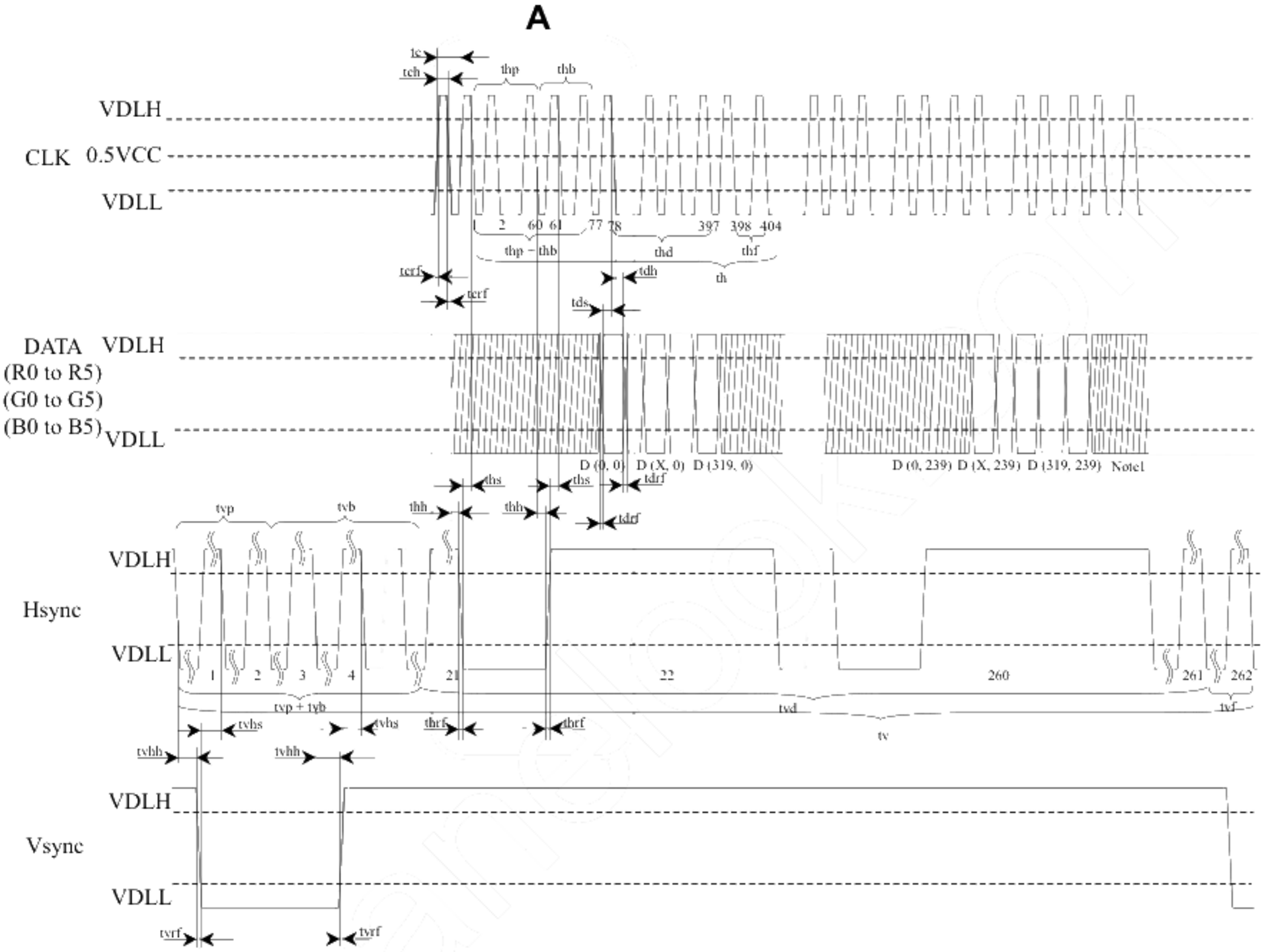
Note2: This diagram indicates virtual signal for set up to timing.

Note3: Customer should be inputted synchronized signals (Hsync, Vsync) in addition to DE signal to this product, when it is worked in DE mode. Synchronized signals are used for DE/Fixed mode detection.

Note4: See "4.9.5 Detailed VGA input signal timing chart for fixed mode" and "4.9.6 Detailed VGA input signal timing chart for DE mode" for numeration of pulse.

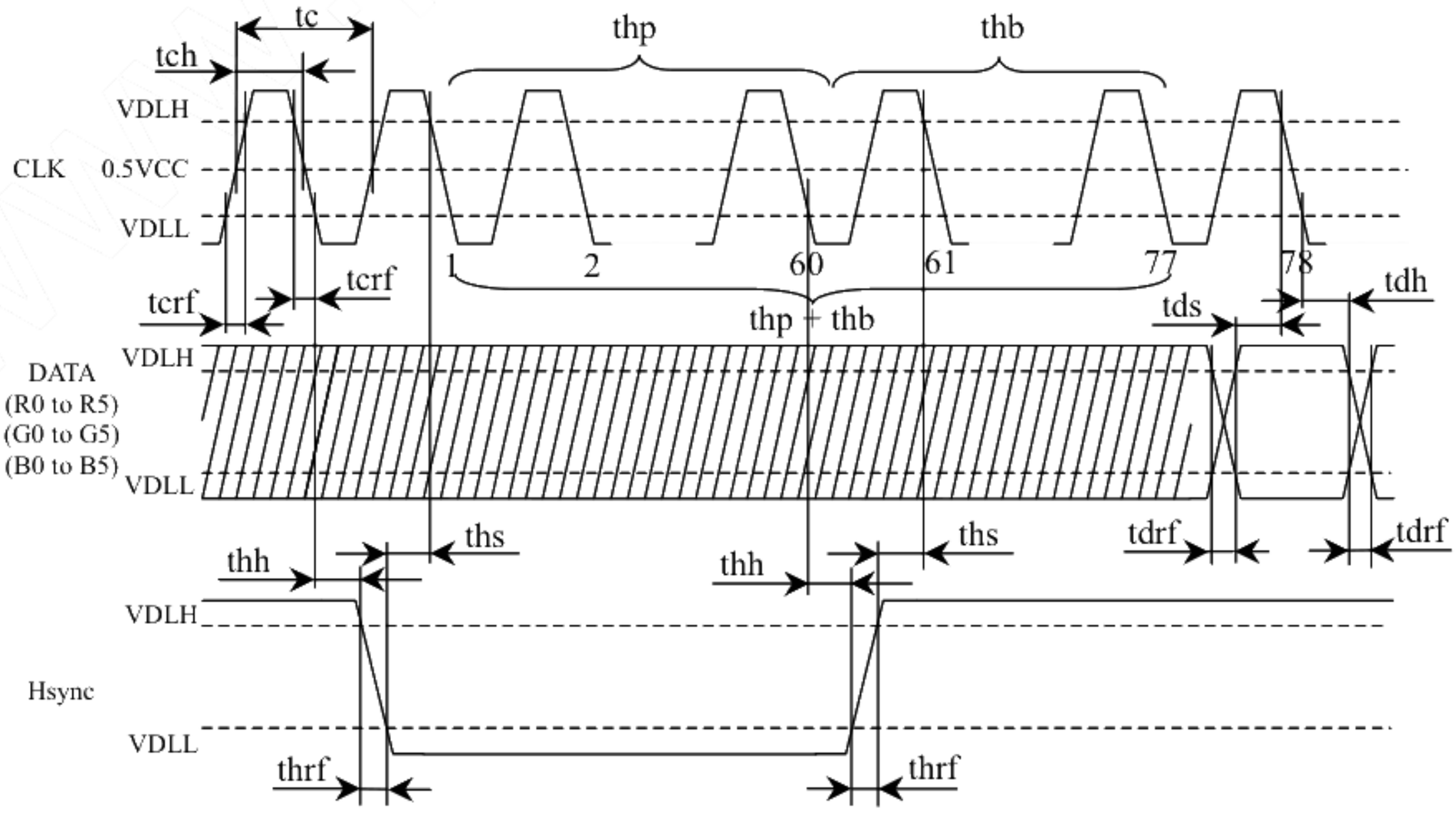
4.9.3 Detailed QVGA input signal timing chart for fixed mode

• Outline chart



Note1: X is data number from 1 to 318. See "4.8.1 QVGA display mode".

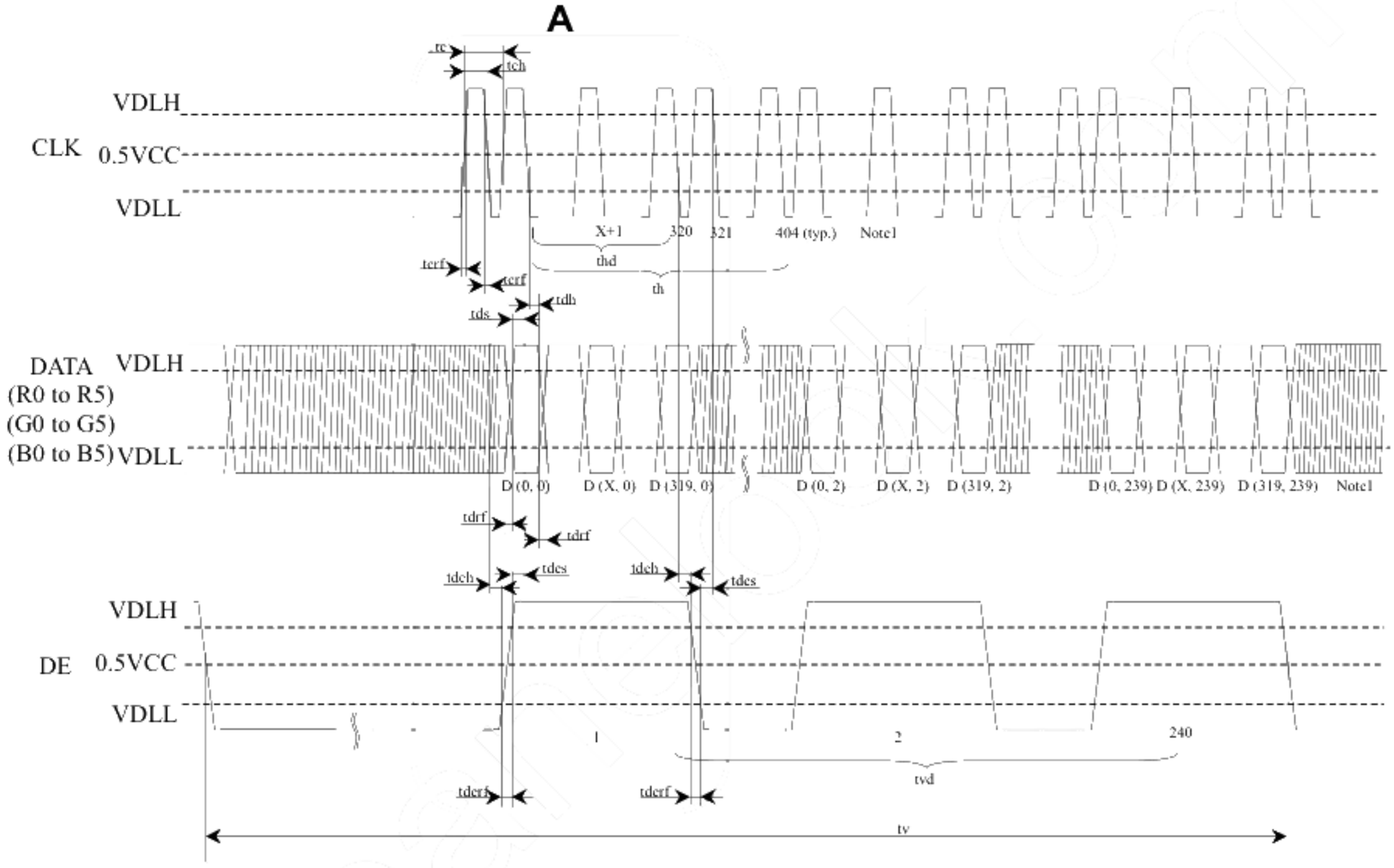
• Detail of **A** part



4.9.4 Detailed QVGA input signal timing chart for DE mode

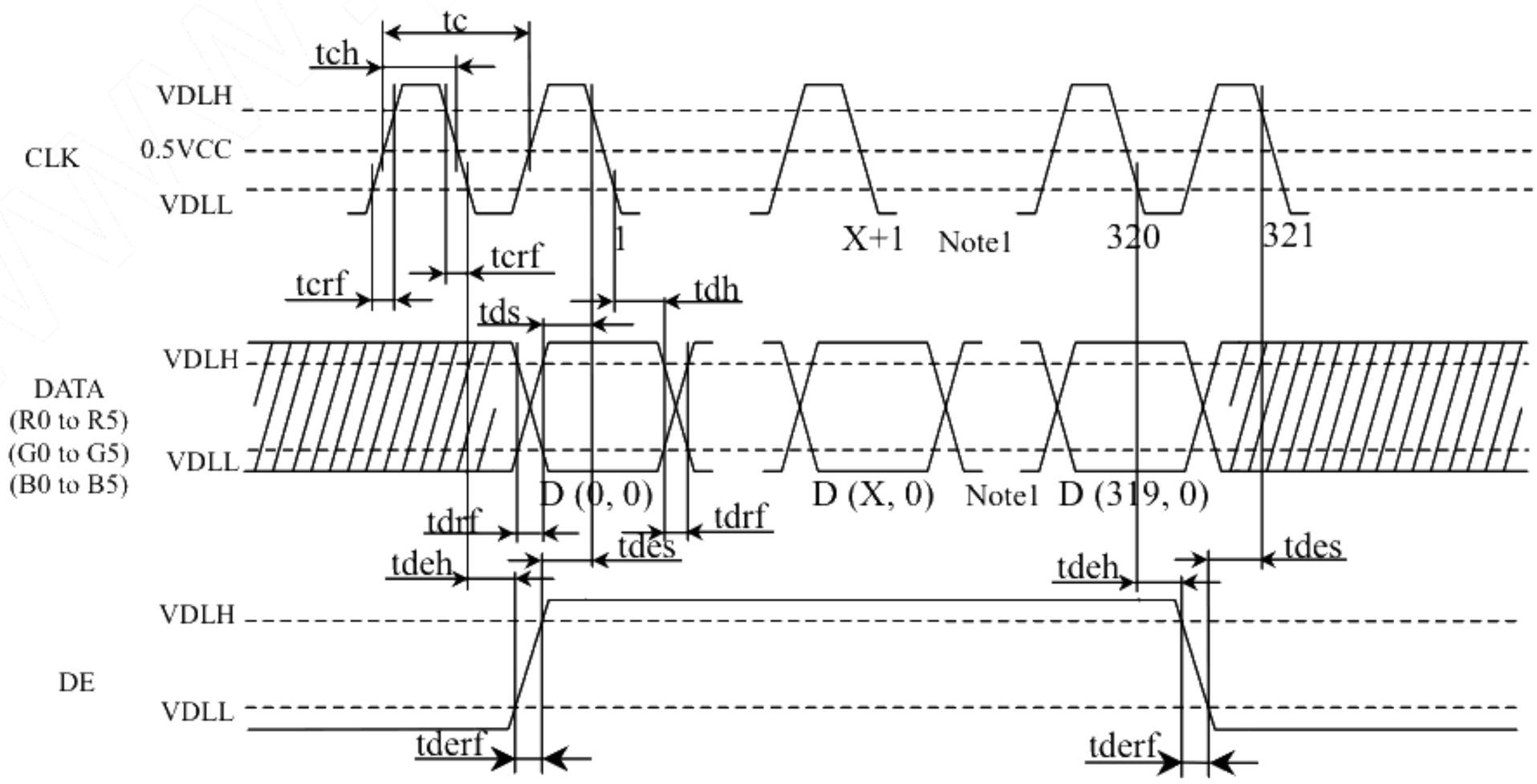
Customer should be inputted synchronized signals (See "4.9.3 Detailed QVGA input signal timing chart for fixed mode".) in addition to DE signal to this product, when it is worked in DE mode. Synchronized signals are used for DE/Fixed mode detection.

• Outline chart



Note1: X is data number from 1 to 318. See "4.8.1 QVGA display mode".

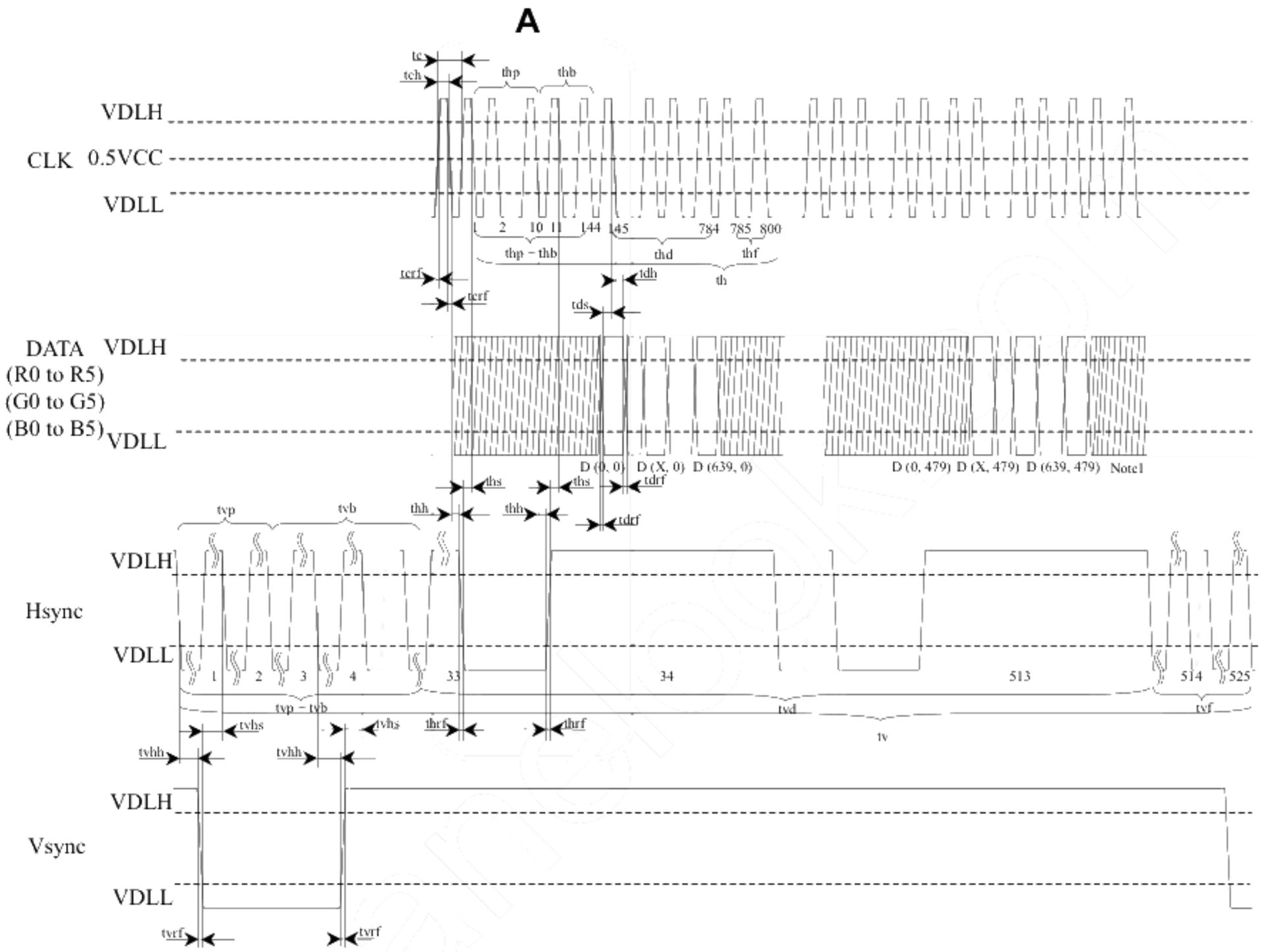
• Detail of **A** part



Note1: X is data number from 1 to 318. See "4.8.1 QVGA display mode".

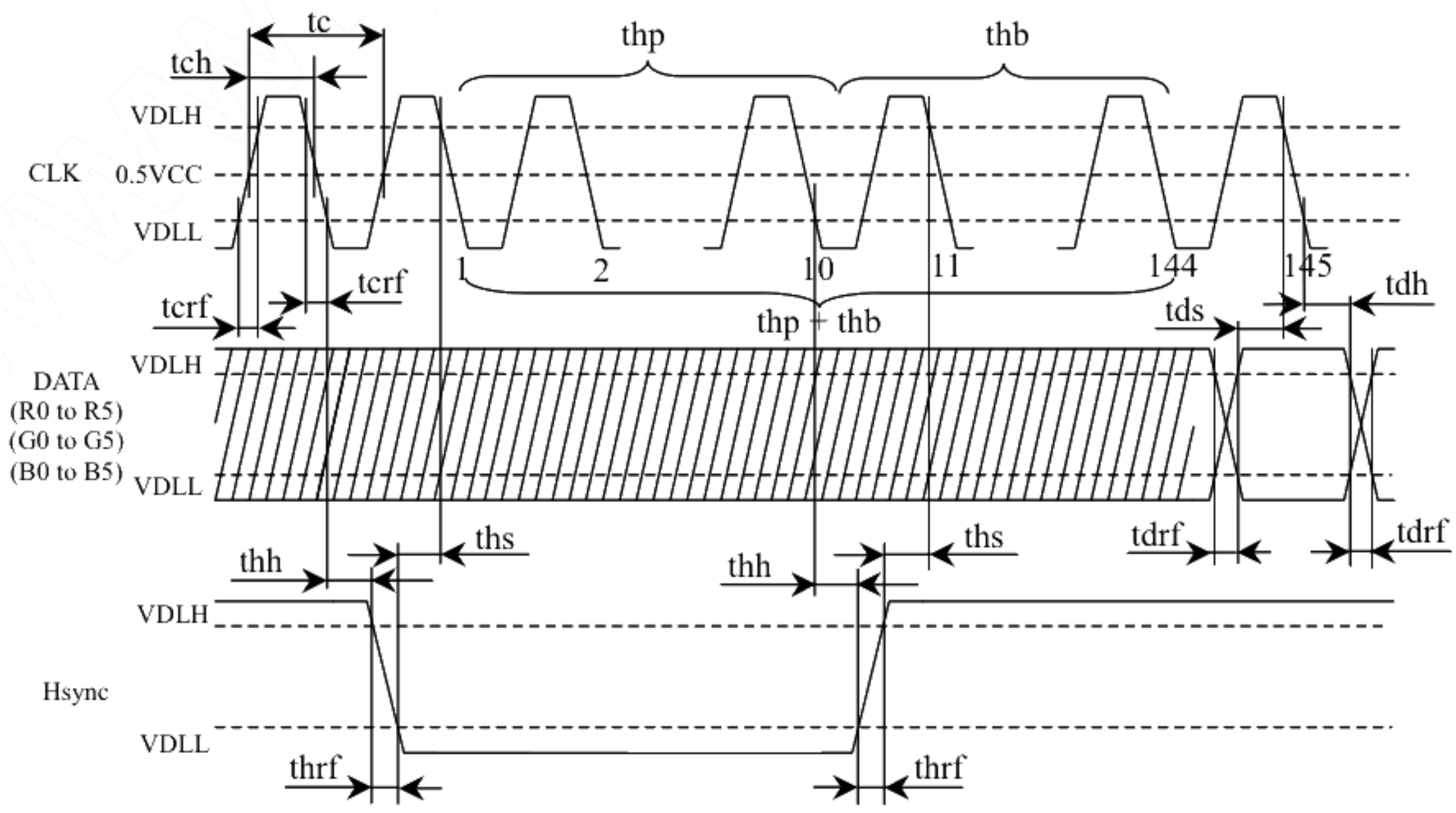
4.9.5 Detailed VGA input signal timing chart for fixed mode

• Outline chart



Note1: X is data number from 1 to 638. See "4.8.2 VGA display mode".

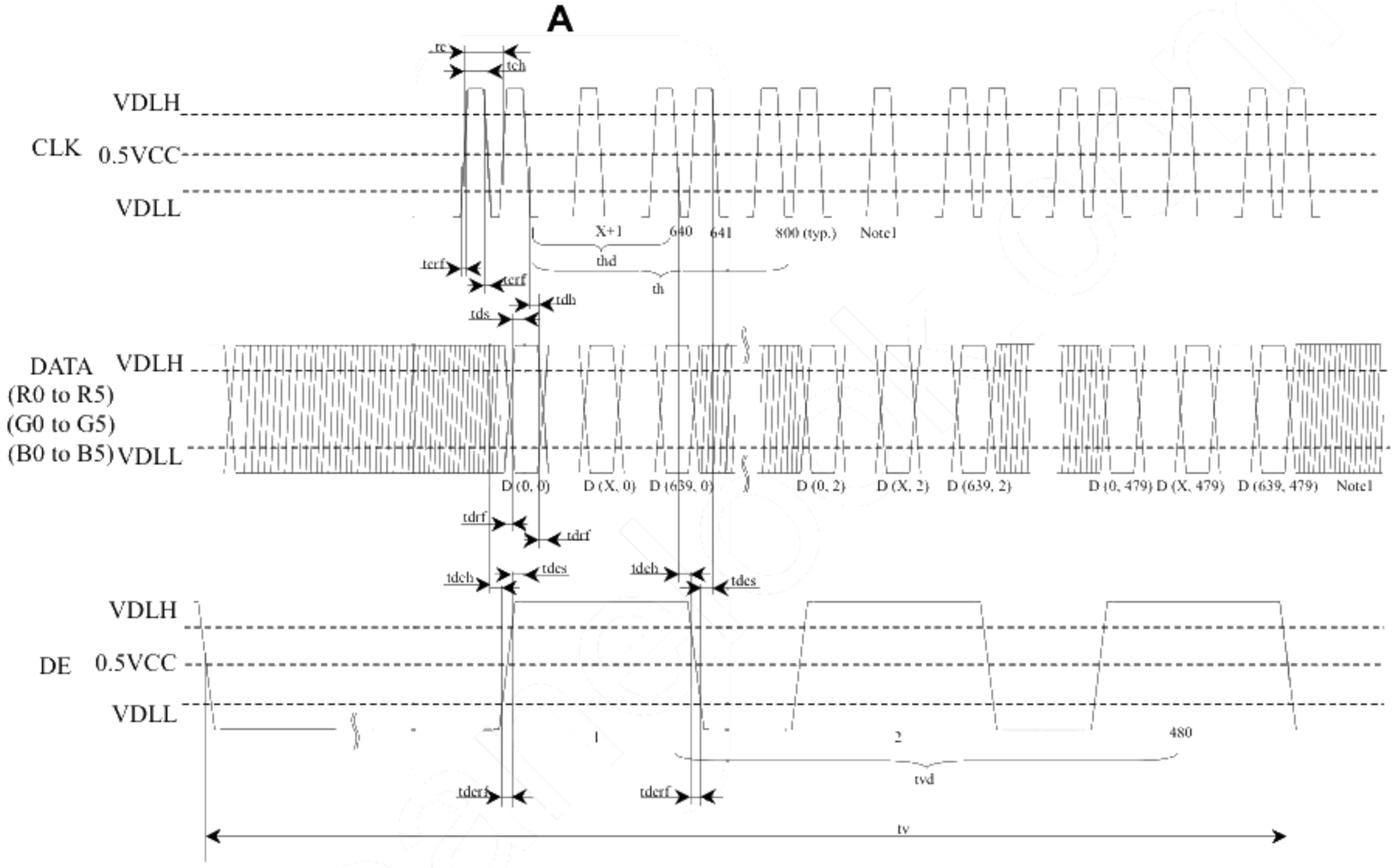
• Detail of **A** part



4.9.6 Detailed VGA input signal timing chart for DE mode

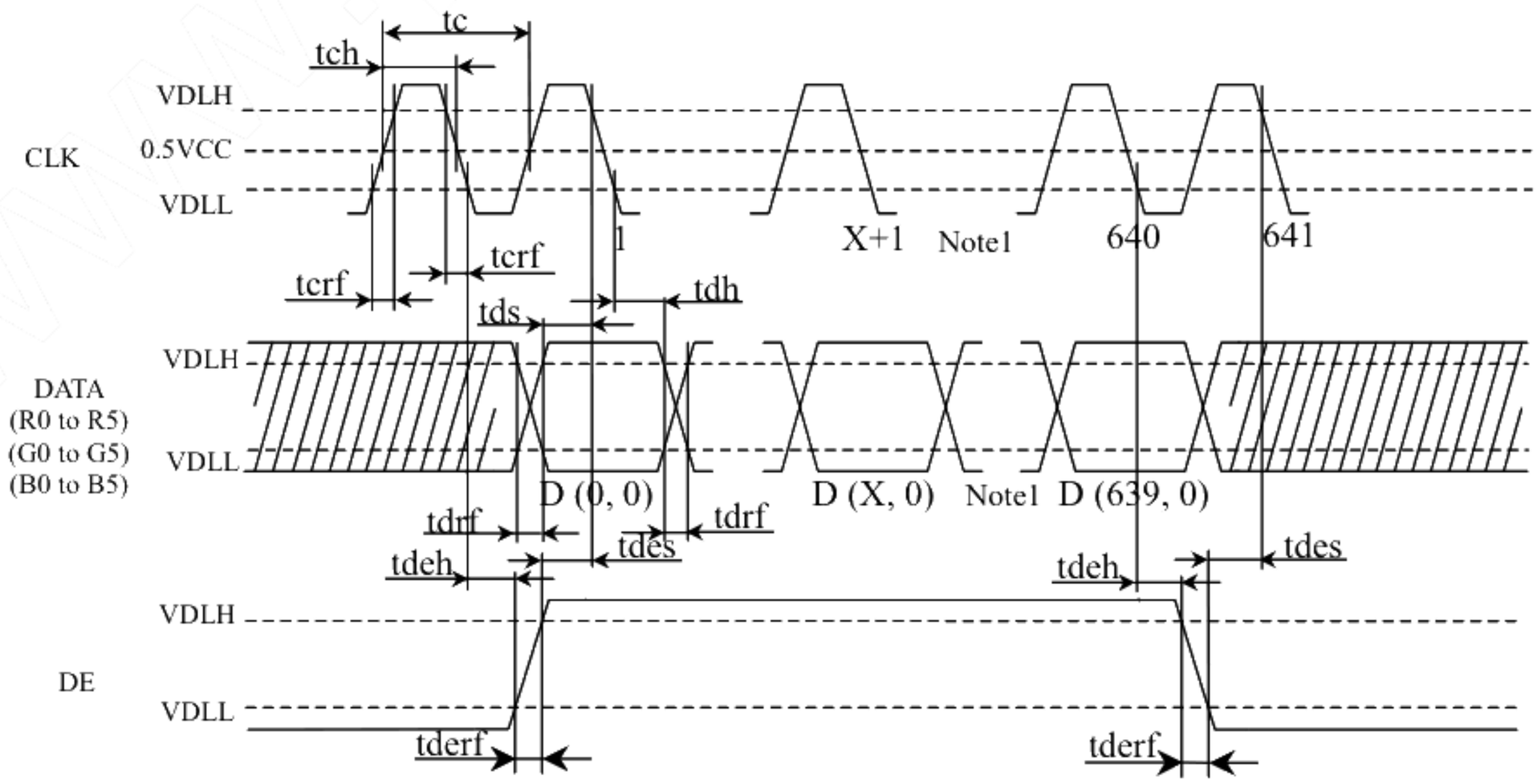
Customer should be inputted synchronized signals (See "4.9.5 Detailed VGA input signal timing chart for fixed mode".) in addition to DE signal to this product, when it is worked in DE mode. Synchronized signals are used for DE/Fixed mode detection.

• Outline chart



Note1: X is data number from 1 to 638. See "4.8.2 VGA display mode".

• Detail of **A** part



Note1: X is data number from 1 to 638. See "4.8.2 VGA display mode".

4.9.7 Timing characteristics for QVGA display mode

• Common to DE mode and fixed mode

Parameter			Symbol	Min.	Typ.	Max.	Unit	Remarks
CLK	Frequency		tcf	5.0	6.4	7.0	MHz	157.5 ns (typ.) Note1
	Duty		tcd	0.4	-	0.6	-	Note1
	Rise time, Fall time		tcrf	-	-	10	ns	-
DATA	CLK-DATA	Setup time	tds	5	-	-	ns	
		Hold time	tdh	10	-	-	ns	
	Rise time, Fall time		tdrf	-	-	10	ns	

Note1: Definition of parameters is as follows.

tcf = 1/tc, tcd = tch/tc = tch×tcd

• Fixed mode

Parameter			Symbol	Min.	Typ.	Max.	Unit	Remarks
Hsync	Cycle		th	57.7	63.5	80.8	μs	15.7 kHz (typ.)
					404		CLK	Note1
	Display period		thd		320		CLK	
	Front-porch		thf		7		CLK	
	Pulse width		thp	3	-	76	CLK	
	Back-porch		thb	1	-	74	CLK	
	Total of pulse width and back-porch		thp + thb		77		CLK	Note1, Note2
	CLK- Hsync	Setup time	ths	5	-	-	ns	-
		Hold time	thh	10	-	-	ns	
	Rise time, Fall time		thrf	-	-	10	ns	
Vsync	Cycle		tv	15.1	16.6	21.2	ms	60.1 Hz (typ.)
					262		H	Note1
	Display period		tvd		240		H	
	Front-porch		tvf		1		H	
	Pulse width		tvp	2	-	20	H	
	Back-porch		tvb	1	-	19	H	
	Total of pulse width and back-porch		tvp + tvb		21		H	Note1, Note2
	Vsync-Hsync	Setup time	tvhs	1	-	-	CLK	Note1
		Hold time	tvhh	10	-	-	ns	-
	Rise time, Fall time		tvrf	-	-	10	ns	

Note1: Definition of parameters is as follows.

tc = 1CLK, th = 1H

Note2: Keep tvp + tvb and thp + thb within the table. If it is out of specification, display position will be shifted to right/left side or up/down.

• DE mode

Parameter			Symbol	Min.	Typ.	Max.	Unit	Remarks
DE Note1	Horizontal	Cycle	th	331	404	-	CLK	Note2
		Display period	thd		320		CLK	
	Vertical (One frame)	Cycle	tv	224	262	-	H	
		Display period	tvd		240		H	
	CLK-DE	Setup time	tdes	5	-	-	ns	-
		Hold time	tdeh	10	-	-	ns	
	Rise time, Fall time		tderf	-	-	10	ns	

Note1: Customer should be inputted synchronized signals (See fixed mode in "4.9.7 Timing characteristics for QVGA display mode".) in addition to DE signal to this product, when it is worked in DE mode. Synchronized signals are used for DE/Fixed mode detection.

Note2: Definition of parameters is as follows.

tc = 1CLK, th = 1H

4.9.8 Timing characteristics for VGA display mode

• Common to DE mode and fixed mode

Parameter			Symbol	Min.	Typ.	Max.	Unit	Remarks
CLK	Frequency		tcf	-	25.2	-	MHz	39.7 ns (typ.) Note1
	Duty		tcd	-	0.5	-	-	Note1
	Rise time, Fall time		tcrf	-	-	-	ns	-
DATA	CLK-DATA	Setup time	tds	-	-	-	ns	
		Hold time	tdh	-	-	-	ns	
	Rise time, Fall time		tdrf	-	-	-	ns	

Note1: Definition of parameters is as follows.

tcf = 1/tc, tcd = tch/tc = tch×tcd

• Fixed mode

Parameter			Symbol	Min.	Typ.	Max.	Unit	Remarks
Hsync	Cycle		th	-	31.8	-	μs	31.4 kHz (typ.)
					800		CLK	Note1
	Display period		thd		640		CLK	
	Front-porch		thf		16		CLK	
	Pulse width		thp	-	-	-	CLK	
	Back-porch		thb	-	-	-	CLK	
	Total of pulse width and back-porch		thp + thb		144		CLK	Note1, Note2
	CLK- Hsync	Setup time	ths	-	-	-	ns	-
		Hold time	thh	-	-	-	ns	
	Rise time, Fall time		thrf	-	-	-	ns	
Vsync	Cycle		tv	-	16.7	-	ms	59.9 Hz (typ.)
					525		H	Note1
	Display period		tvd		480		H	
	Front-porch		tvf		12		H	
	Pulse width		tvp	-	-	-	H	
	Back-porch		tvb	-	-	-	H	
	Total of pulse width and back-porch		tvp + tvb		33		H	Note1, Note2
	Vsync-Hsync	Setup time	tvhs	-	-	-	CLK	Note1
		Hold time	tvhh	-	-	-	ns	-
	Rise time, Fall time		tvrf	-	-	-	ns	

Note1: Definition of parameters is as follows.

tc = 1CLK, th = 1H

Note2: Keep tvp + tvb and thp + thb within the table. If it is out of specification, display position will be shifted to right/left side or up/down.

• DE mode

Parameter			Symbol	Min.	Typ.	Max.	Unit	Remarks
DE Note1	Horizontal	Cycle	th	-	800	-	CLK	Note2
		Display period	thd		640		CLK	
	Vertical (One frame)	Cycle	tv	-	525	-	H	
		Display period	tvd		480		H	
	CLK-DE	Setup time	tdes	-	-	-	ns	-
		Hold time	tdeh	-	-	-	ns	
	Rise time, Fall time		tderf	-	-	-	ns	

Note1: Customer should be inputted synchronized signals (See fixed mode in "4.9.8 Timing characteristics for VGA display mode".) in addition to DE signal to this product, when it is worked in DE mode. Synchronized signals are used for DE/Fixed mode detection.

Note2: Definition of parameters is as follows.

tc = 1CLK, th = 1H

4.10 OPTICS

4.10.1 Optical characteristics

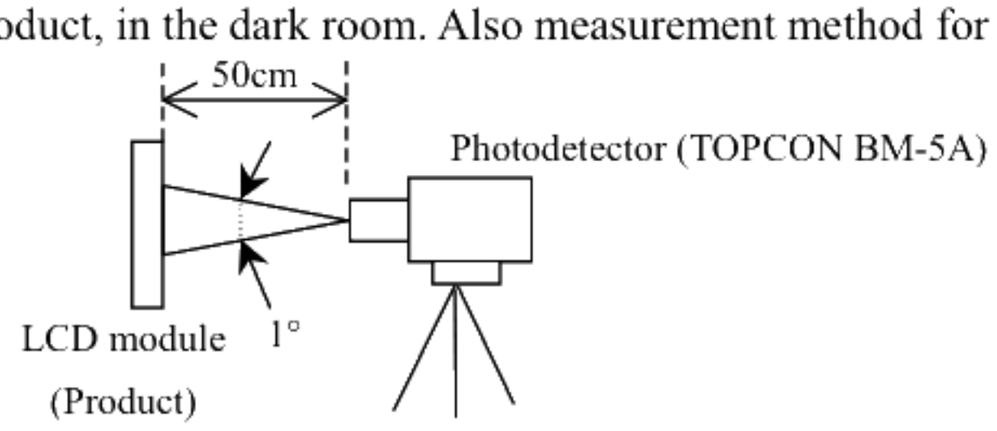
The following characteristics are only applied to QVGA display mode.

Parameter Note1		Condition	Symbol	Min.	Typ.	Max.	Unit	Remarks
Contrast ratio		White/Black at center θR = 0°, θL = 0°, θU = 0°, θD = 0°	CR	320	400	-	-	Note2
Luminance		White at center θR = 0°, θL = 0°, θU = 0°, θD = 0°	L	320	400	-	cd/m^2	-
Luminance uniformity		-	LU	-	1.25	1.35	-	Note3
Chromaticity	White	**x** coordinate	Wx	-	0.305	-	-	Note4
		y coordinate	Wy	-	0.330	-	-	
	Red	**x** coordinate	Rx	-	0.600	-	-	
		y coordinate	Ry	-	0.350	-	-	
	Green	**x** coordinate	Gx	-	0.320	-	-	
		y coordinate	Gy	-	0.560	-	-	
	Blue	**x** coordinate	Bx	-	0.150	-	-	
		y coordinate	By	-	0.130	-	-	
Color gamut		θR = 0°, θL = 0°, θU = 0°, θD = 0° at center, against NTSC color space	C	-	50	-	%	
Response time		White to black	Ton	-	5	15	ms	Note5 Note6
		Black to white	Toff	-	25	50	ms	
Viewing angle	Right	θU = 0°, θD = 0°, CR = 10	θR	-	65	-	°	Note7
	Left	θU = 0°, θD = 0°, CR = 10	θL	-	65	-	°	
	Up	θR = 0°, θL = 0°, CR = 10	θU	-	40	-	°	
	Down	θR = 0°, θL = 0°, CR = 10	θD	-	65	-	°	

Note1: Measurement conditions are as follows.

Ta = 25°C, VCC = 3.3V, IBL = 5.0mArms/lamp, DPSH: Low, DPSV: Low, PNS: Low

Optical characteristics are measured at luminance saturation after 20minutes from working the product, in the dark room. Also measurement method for luminance is as follows.



Note2: See "4.10.2 Definition of contrast ratio".

Note3: See "4.10.3 Definition of luminance uniformity".

Note4: These coordinates are found on CIE 1931 chromaticity diagram.

Note5: Product surface temperature: TopF = 32.5°C

Note6: See "4.10.4 Definition of response times".

Note7: See "4.10.5 Definition of viewing angles".

4.10.2 Definition of contrast ratio

The contrast ratio is calculated by using the following formula.

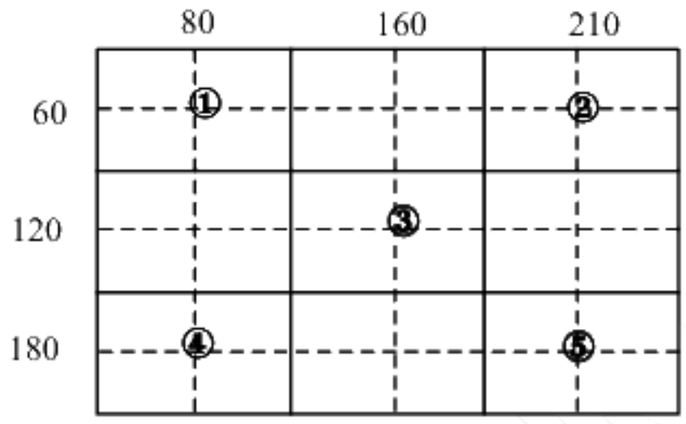
$$\text{Contrast ratio (CR)} = \frac{\text{Luminance of white screen}}{\text{Luminance of black screen}}$$

4.10.3 Definition of luminance uniformity

The luminance uniformity is calculated by using following formula.

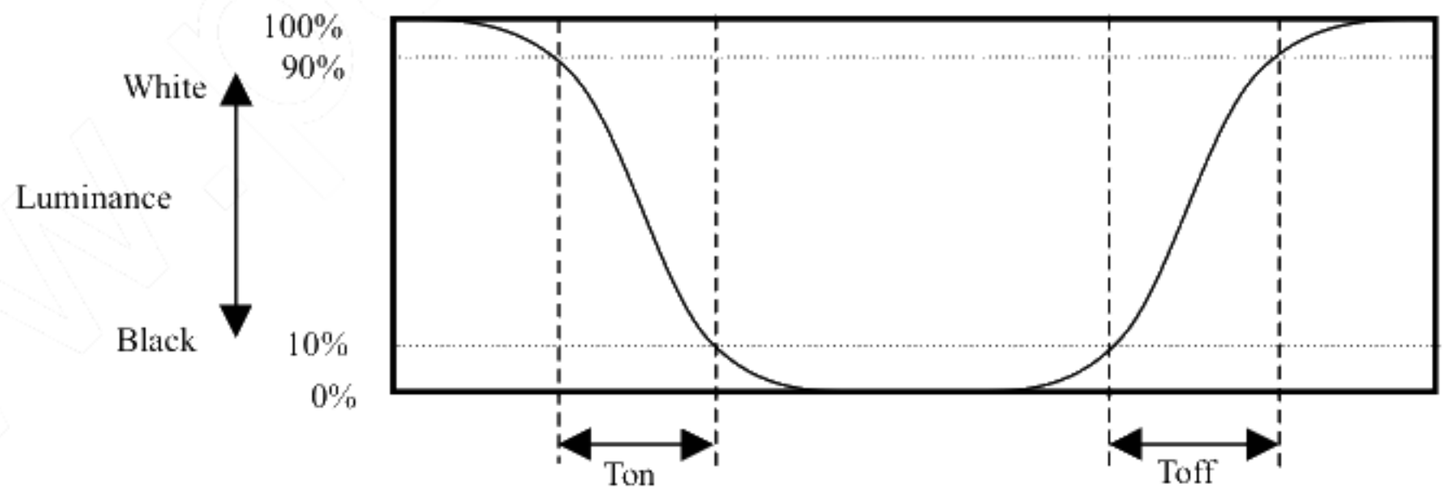
$$\text{Luminance uniformity (LU)} = \frac{\text{Maximum luminance from ① to ⑤}}{\text{Minimum luminance from ① to ⑤}}$$

The luminance is measured at near the 5 points shown below.

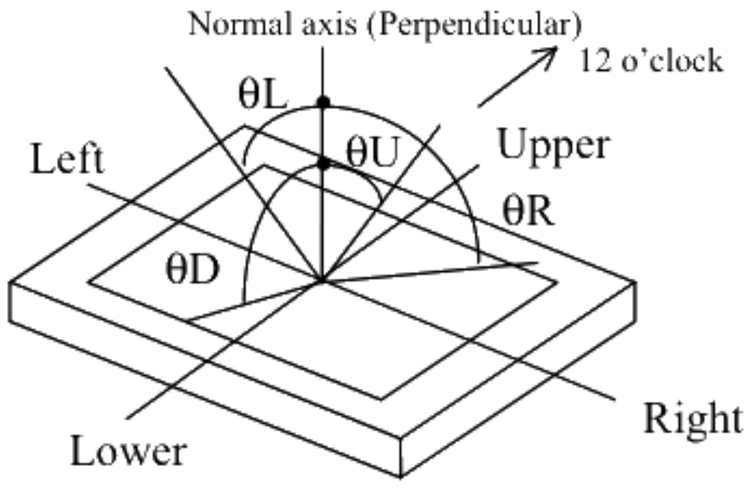


4.10.4 Definition of response times

Response time is measured, the luminance changes from "white" to "black", or "black" to "white" on the same screen point, by photo-detector. Ton is the time it takes the luminance change from 90% down to 10%. Also Toff is the time it takes the luminance change from 10% up to 90% (See the following diagram.).



4.10.5 Definition of viewing angles



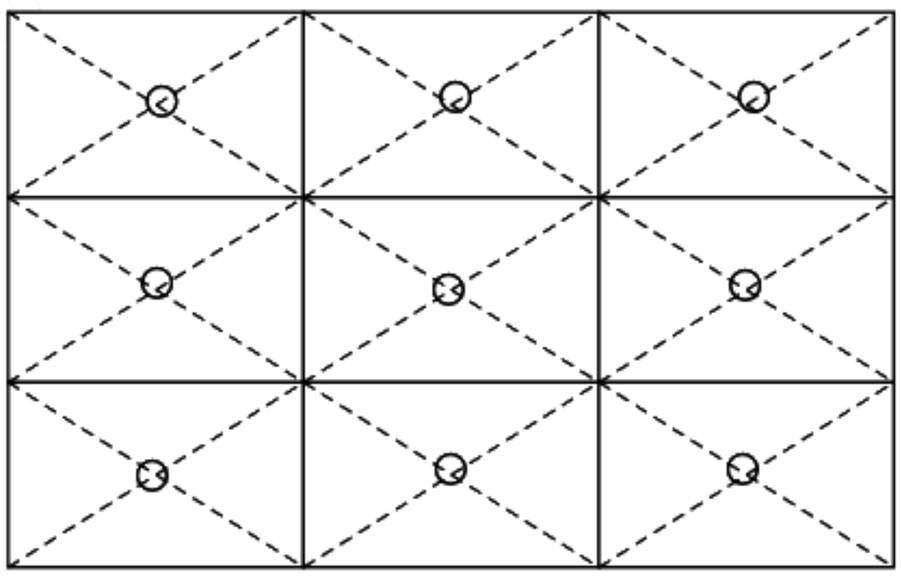
5. RELIABILITY TESTS

The result for reliability tests is only applied to QVGA display mode.

Test item	Condition	Judgement
High temperature and humidity (Operation)	① 55 ± 2°C, RH = 85%, 240hours ② Display data is black.	No display malfunctions Note1
High temperature (Operation)	① 70 ± 2°C, 240hours ② Display data is black.	
Heat cycle (Operation)	① -10 ± 3°C…1hour 70 ± 3°C…1hour ② 50cycles, 4hours/cycle ③ Display data is black.	
Thermal shock (Non operation)	① -30 ± 3°C…30minutes 80 ± 3°C…30minutes ② 100cycles, 1hour/cycle ③ Temperature transition time is within 5 minutes.	
ESD (Operation)	① 150pF, 150Ω, ±10kV ② 9 places on a panel surface Note2 ③ 10 times each places at 1 sec interval	
Dust (Operation)	① Sample dust: No. 15 (by JIS-Z8901) ② 15 seconds stir ③ 8 times repeat at 1 hour interval	
Vibration (Non operation)	① 5 to 200Hz, 29.4m/s^2 ② 10 minute/cycle ③ X, Y direction…2hours ④ Z direction…4hours	No display malfunctions Note1 No physical damages
Mechanical shock (Non operation)	① 980m/ s^2, 11ms ② ±X, ±Y, ±Z direction ③ 3 times each directions	

Note1: Display functions are checked under the same conditions as product inspection.

Note2: See the following figure for discharge points.



6. PRECAUTIONS

6.1 MEANING OF CAUTION SIGNS

The following caution signs have very important meaning. **Be sure to read "6.2 CAUTIONS", after understanding this contents!**

This sign has the meaning that customer will be injured by himself, if customer has wrong operations.

6.2 CAUTIONS

∗ Pay attention to burn injury for the working backlight! It may be over 35°C from ambient temperature.

∗ Do not shock and press the LCD panel and the backlight! Danger of breaking, because they are made of glass. (Shock: To be not greater 980m/s^2 and to be not greater 11ms, Pressure: To be not greater 19.6N)

6.3 ATTENTIONS

6.3.1 Handling of the product

① Take hold of both ends without touch the circuit board when customer pulls out products (LCD modules) from inner packing box. If customer touches it, products may be broken down or out of adjustment, because of stress to mounting parts.

② Do not hook cables nor pull connection cables such as flexible cable and so on, for fear of damage.

③ If customer puts down the product temporarily, the product puts on flat subsoil as a display side turns down.

④ Take the measures of electrostatic discharge such as earth band, ionic shower and so on, when customer deals with the product, because products may be damaged by electrostatic.

⑤ The torque for mounting screws must never exceed 0.29N·m. Higher torque values might result in distortion of the bezel.

⑥ Do not press or rub on the sensitive display surface. If customer clean on the panel surface, NEC Corporation recommends using the cloth with ethanolic liquid such as screen cleaner for LCD.

⑦ Do not push-pull the interface connectors while the product is working, because wrong power sequence may break down the product.

6.3.2 Environment

① Do not operate or store in high temperature, high humidity, dewdrop atmosphere or corrosive gases. Keep the product in antistatic pouch in room temperature, because of avoidance for dusts and sunlight, if customer stores the product.

② Do not operate in high magnetic field. Circuit boards may be broken down by it.

③ Use an original protection sheet on the product surface (polarizer). Adhesive type protection sheet should be avoided, because it may change color or properties of the polarizer.

6.3.3 Characteristics

The following items are neither defects nor failures.

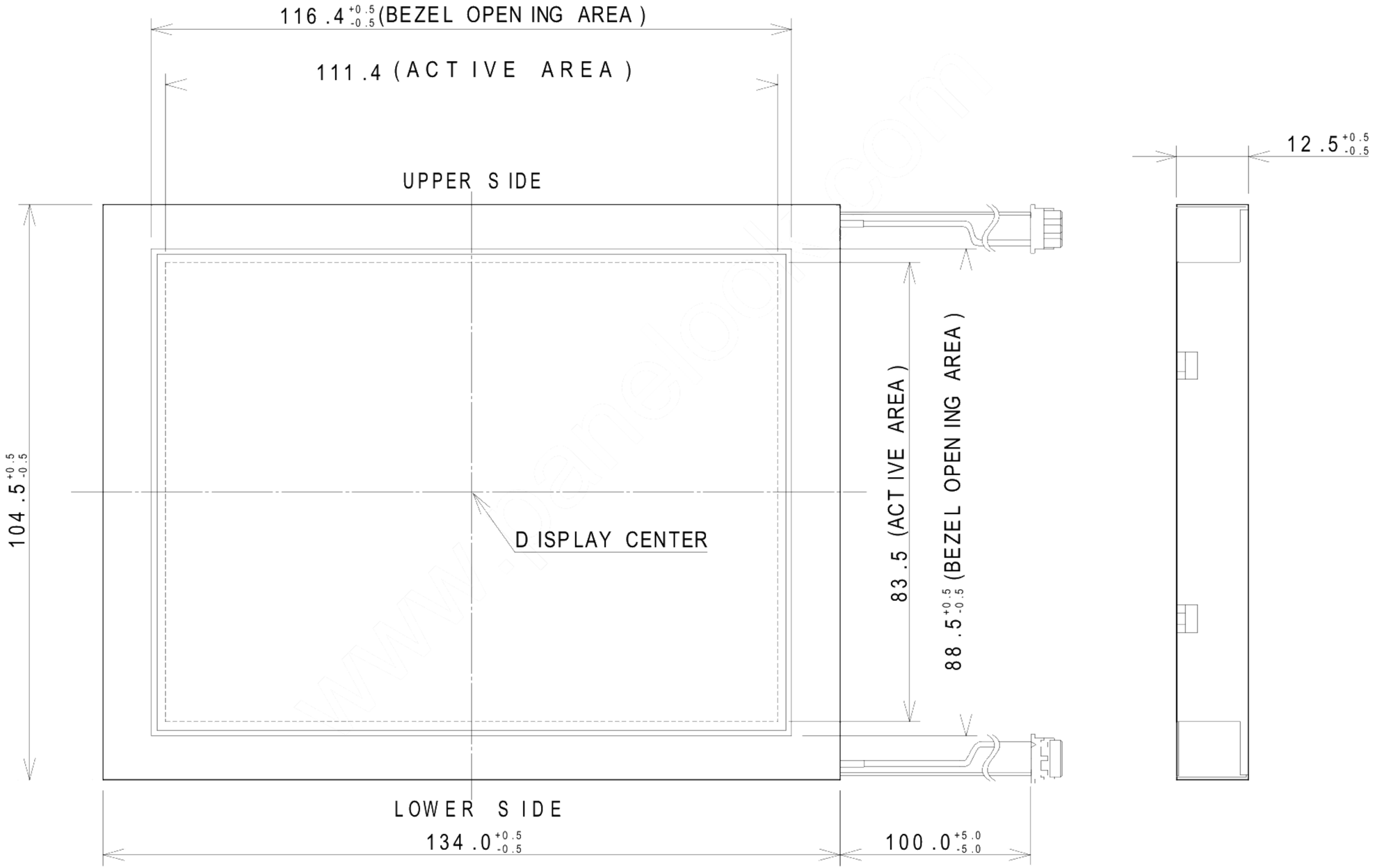
① Response time, luminance and color may be changed by ambient temperature.
② The LCD may be seemed luminance non-uniformity, flicker, vertical seam or small spot by display patterns.
③ Optical characteristics (e.g. luminance, display uniformity, etc.) gradually is going to change depending on operating time, and especially low temperature, because the LCD has cold cathode fluorescent lamps.
④ Do not display the fixed pattern for a long time because it may cause image sticking. Use a screen saver, if the fixed pattern is displayed on the screen.
⑤ The display color may be changed by viewing angle because of the use of condenser sheet in the backlight unit.
⑥ Optical characteristics may be changed by input signal timings.
⑦ The interference noise of input signal frequency for this product's signal processing board and luminance control frequency of customer's backlight inverter may appear on a display. Set up luminance control frequency of backlight inverter so that the interference noise does not appear.

6.3.4 Other

① All GND, backlight inverter ground (GNDB), VCC and backlight inverter power supply voltage (VDDB) terminals should be used without a non-connected line.
② Do not disassemble a product or adjust volume without permission of NEC Corporation.
③ See "REPLACEMENT MANUAL FOR LAMPHOLDER", if customer would like to replace backlight lamps.
④ Pay attention not to insert waste materials inside of products, if customer uses screwnails.

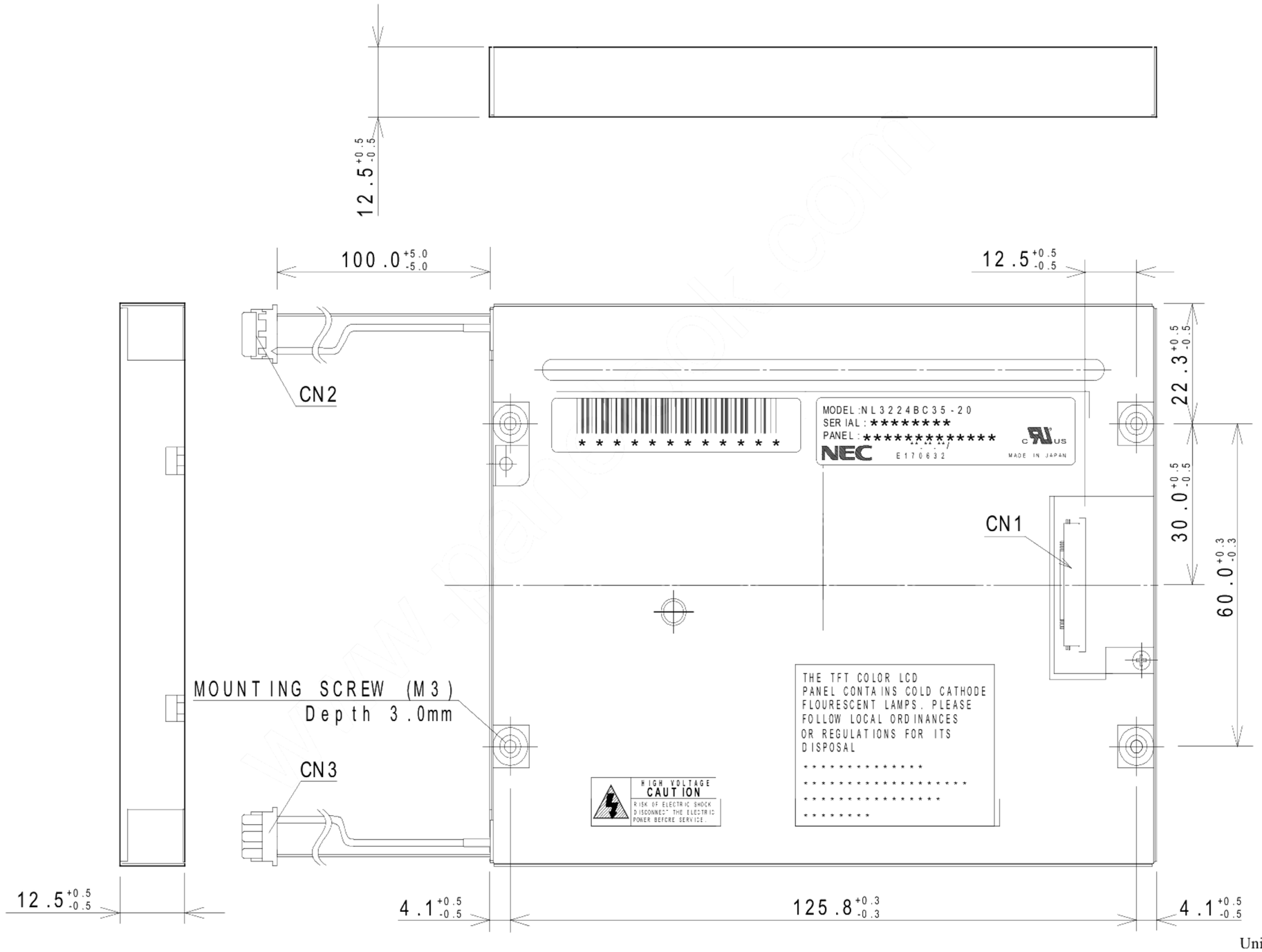
7. OUTLINE DRAWINGS

7.1 FRONT VIEW



Unit: mm

7.2 REAR VIEW



Unit: mm