

Description

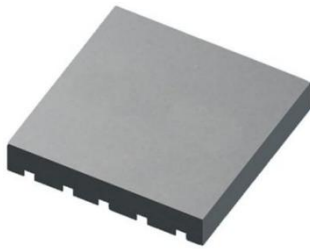
The HTN7G38S007P is an unmatched discrete LDMOS Power Amplifier with 7W saturated output power covering frequency range from 700 - 3800 MHz.


Features

- Operating Frequency Range: 700 - 3800 MHz
- Operating Drain Voltage: +28V
- Saturation Output Power: 7W
- Power Average: 0.76W
- Excellent thermal stability due to low thermal resistance package
- Enhanced robustness design without device degradation
- Internally integrated enhanced ESD design

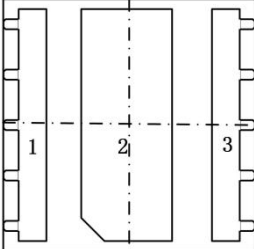
Applications

- CDMA
- W-CDMA
- GSM EDGE
- MC-GSM
- TDD/FDD LTE
- WiMAX



PDFN5X5 

Power Dual Flat pack No Lead



Bottom View
Terminal No.
1: Gate
2: Source
3: Drain

Note: Exposed backside of the package is the source terminal for the transistor

Pin Connections

Ordering Information

Part Number	Description
HTN7G38S007P	Reel Package
HTN7G38S007PEVB	2110 - 2170 MHz EVB
HTN7G38S007PEVB1	2620 - 2690 MHz EVB
HTN7G38S007PEVB2	3300 - 3400 MHz EVB

Typical Performance

RF Characteristics (CW)

Freq (MHz)	Gain (dB)	P1dB (dBm)	Eff (%)@ P1dB (dBm)	P3dB (dBm)	Eff (%)@ P3dB (dBm)
2110	19.4	38.9	55.1	39.5	56.2
2140	19.5	38.7	54.7	39.4	56.0
2170	19.3	38.6	53.6	39.4	55.1
3700	14.8	37.26	43.96	38.53	47.55
3800	15.3	36.40	41.04	38.27	47.21

Test conditions unless otherwise noted: 25 °C, VDD = +28Vdc, IDQ= 70mA test on HOTLO Application Board

Freq (MHz)	Gain (dB)	P1dB (dBm)	Eff (%)@ P1dB (dBm)	P3dB (dBm)	Eff (%)@ P3dB (dBm)
3300	14.8	37.7	43.2	38.8	46.8
3350	14.5	37.5	43.6	38.7	47.6
3400	14.3	37.6	45.1	38.7	48.3

Test conditions unless otherwise noted: 25 °C, VDD = +28Vdc, IDQ= 80mA test on HOTLO Application Board

RF Characteristics (Pulsed CW)

Freq (MHz)	Gain (dB)	P1dB (dBm)	Eff (%)@ P1dB (dBm)	P3dB (dBm)	Eff (%)@ P3dB (dBm)
3700	14.6	38.05	46.01	38.93	48.08
3800	15.2	37.47	46.11	38.69	48.33

Test conditions unless otherwise noted: 25 °C, VDD = +28Vdc, IDQ=70mA, PW = 100us, DC= 10% test on HOTLO Application Board

RF Characteristics (WCDMA)

Freq (MHz)	Gain (dB)	Eff (%)	ACPR* @5MHz (dBc)	IRL (dB)
2110	19.2	19.2	-46.4	12
2140	19.3	19.2	-45.6	18
2170	19.1	18.7	-45.2	16

Test conditions unless otherwise noted: 25 °C, VDD = +28Vdc, IDQ= 100mA, PAVG = 28.8 dBm (0.76W), 1C-WCDMA 5MHz Signal, 9.9 dB PAR @ 0.01% CCDF test on HOTLO Application Board

**Uncorrected DPD*

Freq (MHz)	Gain (dB)	Eff (%)	ACPR* @5MHz (dBc)	IRL (dB)
3300	14.8	16.4	-47.0	9.1
3350	14.4	17.0	-47.6	8.9
3400	14.2	17.4	-47.1	8.8

Test conditions unless otherwise noted: 25 °C, VDD = +28Vdc, IDQ= 80mA, PAVG = 28.8 dBm (0.76W), 1C-WCDMA 5MHz Signal, 9.9 dB PAR @ 0.01% CCDF test on HOTLO Application Board

**Uncorrected DPD*

Freq (MHz)	Gain (dB)	Eff (%)	ACPR* @5MHz (dBc)	IRL (dB)
3700	14.6	18.1	-44.4	11.8
3800	15.2	18.7	-43.0	11.4

Test conditions unless otherwise noted: 25 °C, VDD = +28Vdc, IDQ= 80mA, PAVG = 28.8 dBm (0.76W), 1C-WCDMA 5MHz Signal, 9.9 dB PAR @ 0.01% CCDF test on HOTLO Application Board

**Uncorrected DPD*

RF Characteristics (LTE)

Freq (MHz)	Gain (dB)	Eff (%)	ACPR (dBc)*	IRL (dB)
3310	14.8	17.2	-48.2	9.1
3350	14.4	17.7	-48.1	8.9
3390	14.2	18.1	-47.1	8.8

Test conditions unless otherwise noted: 25 °C, VDD = +12Vdc, IDQ= 80mA, PAVG = 28.8 dBm (0.76W), FDD LTE 20MHz DL Signal, 10 dB PAR @ 0.01% CCDF test on HOTLO Application Board

**Uncorrected DPD*

Freq (MHz)	Gain (dB)	Eff (%)	ACPR (dBc)*	IRL (dB)
3700	14.6	17.9	-42.2	11.8
3800	15.2	18.3	-41.0	11.4

Test conditions unless otherwise noted: 25 °C, VDD = +12Vdc, IDQ= 70mA, PAVG = 28.8 dBm (0.76W), FDD LTE 20MHz DL Signal, 10 dB PAR @ 0.01% CCDF test on HOTLO Application Board

**Uncorrected DPD*

Absolute Maximum Ratings

Parameter	Range/Value	Unit
Drain voltage (V _{DSS})	-0.5, +65	V
Gate voltage (V _{GS})	-5 to +10	V
Operation voltage (V _{DD})	+0 to +28	V
Storage Temperature (T _{STG})	-55 to +150	°C
Case Temperature (T _c)	-40 to +150	°C
Junction Temperature (T _J)	-40 to +225	°C

Electrical Specification

DC Characteristics

Parameter	Conditions	Min	Typ	Max	Unit
Breakdown Voltage V _{(BR)DSS}	V _{gs} =0V, I _{ds} =8.4uA	65	-	-	V
Gate-Source Threshold Voltage V _{GS(th)}	V _{ds} =V _{gs} , I _{ds} =8.4uA	-	1.4	-	V
Drain Leakage Current I _{DSS}	V _{gs} =0V, V _{ds} =65V	-	-	1.4	uA
Gate Leakage Current I _{GSS}	V _{gs} =5V, V _{ds} =0V	-	-	140	nA

Load Mismatch Test

Condition	Test Result
VSWR=10:1, at all Phase Angles, VDD = +28Vdc, IDQ= 70mA, CW signal Pout = 40 dBm (3dB input Overdrive from P3dB) @2140 MHz test on HOTLO Application Board	No Device Degradation

Thermal Information

Parameter	Condition	Value (Typ)	Unit
Thermal Resistance Junction to Case (R _{TH})	T _{CASE} = 50°C, VDD = +28Vdc, IDQ= 70mA, CW signal 7W	2.9	°C /W

RF Characteristics (WCDMA)

Parameter	Conditions	Min	Typ.	Max	Unit
Frequency		2140			MHz
Gain	PAVG = 28.8dBm	-	19.3	-	dB
Eff	PAVG = 28.8dBm	-	19.2	-	%
ACPR@5MHz*	PAVG = 28.8dBm	-	-45.6	-	dBc

Test conditions unless otherwise noted: 25 °C, VDD = +28Vdc, IDQ= 70mA, PAVG = 28.8 dBm (0.76W), 1C-WCDMA 5MHz Signal, 9.9 dB PAR @ 0.01% CCDF test on HOTLO Application Board

*Uncorrected DPD, measured in 3.84MHz Channel Bandwidth @ ±5MHz Offset

RF Characteristics (CW)

Parameter	Conditions	Min	Typ.	Max	Unit
P1dB	2140 MHz	-	38.9	-	dB
AM/PM (\emptyset)	2110-2170 MHz@P3dB	-	18.1	-	$^{\circ}$
VBWres	(IMD Third Order Inter modulation Inflection Point)	-	90	-	MHz
Gain Flatness	2110-2170 MHz@60 MHz	-	0.3	-	dB

Test conditions unless otherwise noted: 25 °C, VDD = +28Vdc, IDQ= 70mA test on HOTLO Application Board

Load Pull Performance for Maximum Power (P1dB/P3dB)

Test conditions unless otherwise noted: 25 °C, VDD = +28Vdc, IDQ= 70mA, PW = 40us, DC= 4%

Max Output Power P1dB						
Freq (MHz)	Z_source (Ω)	Z_load [1] (Ω)	Gain (dB)	P1dB (dBm)	P1dB (W)	Eff (%)
920	1.40+j*8.88	33.21+j*2.89	24.89	41.02	12.65	62.60
1400	1.42+j*3.55	26.36+j*3.33	22.02	39.95	9.89	59.478
1800	0.81+j*2.15	17.20+j*5.22	21.36	39.86	9.68	58.36
2110	0.83-j*0.95	11.00+j*6.41	20.79	39.88	9.73	58.09
2300	0.95-j*2.25	10.12+j*7.20	20.17	39.52	8.95	54.08
2690	1.02-j*3.11	9.00+j*3.34	18.89	39.37	8.65	52.99
3400	2.52-j*6.89	6.82-j*1.04	15.88	38.89	7.74	49.02

[1] Load impedance for optimum P1dB pout

Max Output Power P3dB						
Freq (MHz)	Z_source (Ω)	Z_load [2] (Ω)	Gain (dB)	P3dB (dBm)	P3dB (W)	Eff (%)
920	1.40+j*8.88	32.23+j*2.82	24.95	41.84	15.28	65.65
1400	1.42+j*3.55	27.14+j*4.17	22.08	40.82	12.08	62.38
1800	0.81+j*2.15	15.16+j*6.23	21.80	40.82	12.11	61.47
2110	0.83-j*0.95	12.35+j*6.26	20.61	40.65	11.61	59.40

2300	0.95-j*2.25	11.73+j*6.54	19.82	40.37	10.89	54.23
2690	1.02-j*3.11	12.05+j*4.01	18.81	40.32	10.76	54.91
3400	2.52-j*6.89	7.14-j*1.44	16.02	39.82	9.59	49.12

[2] Load impedance for optimum P3dB pout

Load Pull Performance for Maximum Efficiency (P1dB/P3dB)

Test conditions unless otherwise noted: 25 °C, VDD = +28Vdc, IDQ= 70mA, PW = 40us, DC= 4%

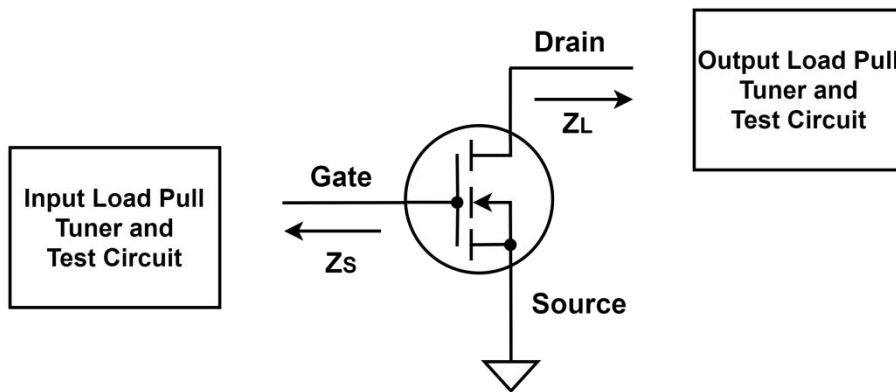
Max Efficiency P1dB						
Freq (MHz)	Z_source (Ω)	Z_load [1] (Ω)	Gain (dB)	P1dB (dBm)	P1dB (W)	Eff (%)
920	1.40+j*8.88	18.64+j*32.81	27.42	38.41	6.93	73.88
1400	1.42+j*3.55	13.42+j*26.48	25.16	36.80	4.79	71.48
1800	0.81+j*2.15	6.01+j*16.72	24.94	36.25	4.22	69.48
2110	0.83-j*0.95	5.77+j*12.95	23.30	37.46	5.57	68.35
2300	0.95-j*2.25	5.26+j*11.98	22.27	37.52	5.65	61.92
2690	1.02-j*3.11	5.47+j*7.03	20.64	37.90	6.17	60.21
3400	2.52-j*6.89	3.96-j*0.85	16.62	38.34	6.82	51.06

[1] Load impedance for optimum P1dB efficiency

Max Efficiency P3dB						
Freq (MHz)	Z_source (Ω)	Z_load [2] (Ω)	Gain (dB)	P3dB (dBm)	P3dB (W)	Eff (%)
920	1.40+j*8.88	25.74+j*32.68	27.26	39.79	9.53	74.58
1400	1.42+j*3.55	13.71+j*25.47	25.29	38.30	6.76	72.12
1800	0.81+j*2.15	7.46+j*14.94	25.02	38.55	7.16	70.92
2110	0.83-j*0.95	5.51+j*12.69	23.36	38.15	6.53	69.55
2300	0.95-j*2.25	4.81+j*11.90	22.36	38.01	6.32	62.29

2690	$1.02-j*3.11$	$6.29+j*6.60$	20.35	39.10	8.13	60.54
3400	$2.52-j*6.89$	$4.11-j*0.97$	16.58	39.23	8.38	51.96

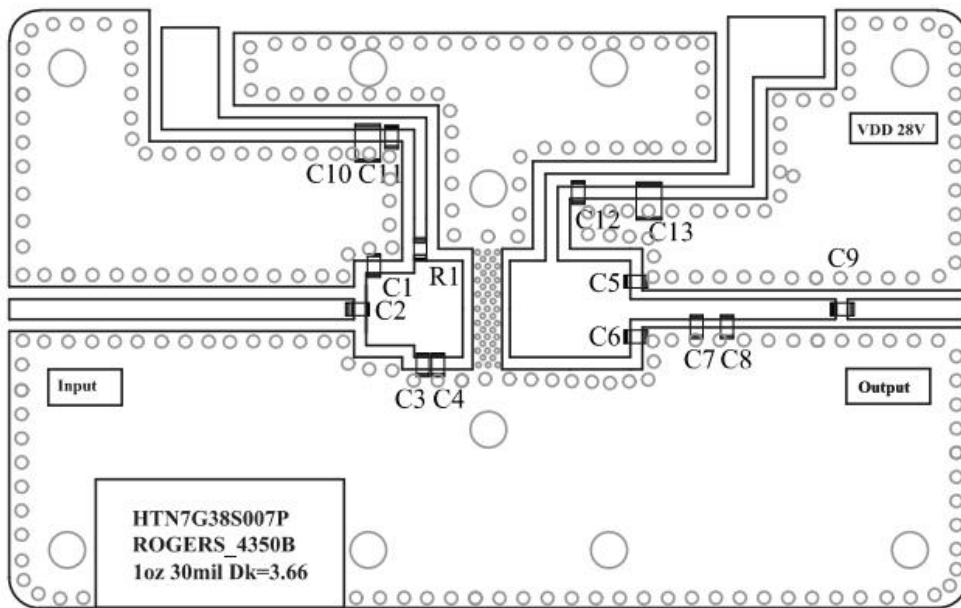
[2] Load impedance for optimum P3dB efficiency



Z_{source} : Measured impedance presented to the input of the device at the package reference plane

Z_{load} : Measured impedance presented to the output of the device at the package reference plane

HTN7G38S007P 2110- 2170 MHz Reference Design



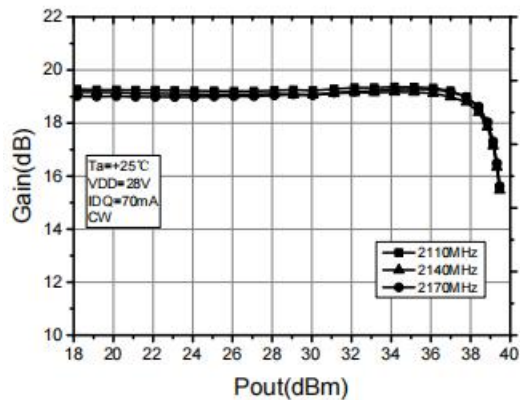
EVB Layout

Bill of Materials (BoM) - HTN7G38S007P 2110- 2170 MHz Reference Design

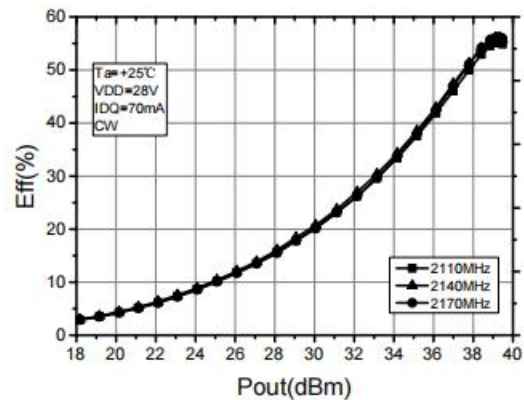
Reference	Value	Description	Manufacturer	P/N
Q1	-	20W, 700 - 3800 MHz LDMOS PA	Holto	HTN7G38S007P

C1	0p3F	MLCC	ATC	600S0R3BT260XT
C2,C9,C11,C12	8p2F	MLCC	ATC	600S8R2BT260XT
C3	2p2F	MLCC	ATC	600S2R2BT260XT
C4	1pF	MLCC	ATC	600S1R0BT260XT
C5	3pF	MLCC	ATC	600S3R0BT260XT
C6	1p5F	MLCC	ATC	600S1R5BT260XT
C7	1p8F	MLCC	ATC	600S1R8BT260XT
C8	1p2F	MLCC	ATC	600S1R2BT260XT
C10,C13	10uF/50V	MLCC	-	1210
R1	10Ω/0603	Thick Film Resistor	-	-
PCB	Rogers4350B (er = 3.66), 20 mil (0.508 mm), 35 μm (1oz)			

Performance Plots 2110- 2170 MHz Reference Design

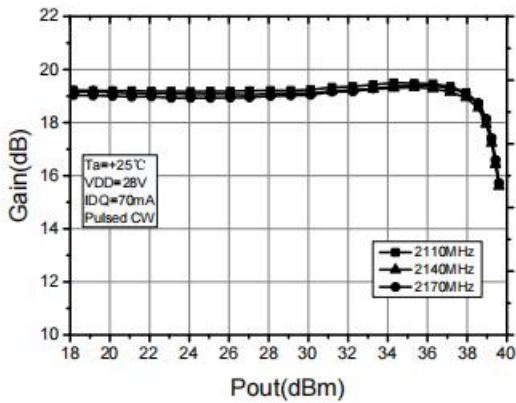


CW, Gain vs Pout

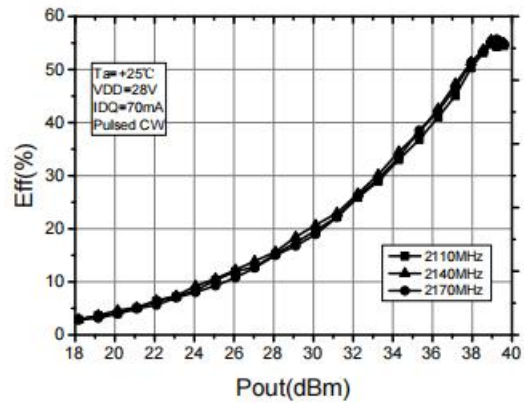


CW, Efficiency vs Pout

Test conditions unless otherwise noted: 25 °C, VDD = +28Vdc, IDQ=70mA test on HOTLO Application Board

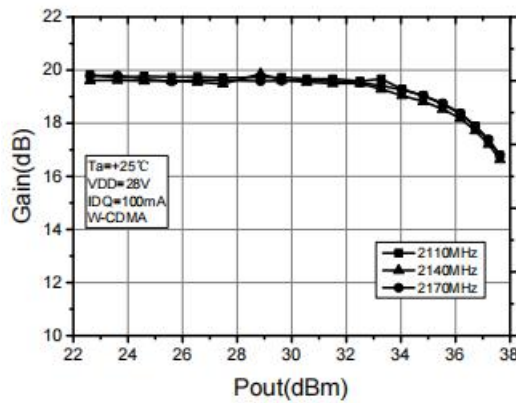


Pulsed CW, Gain vs Pout

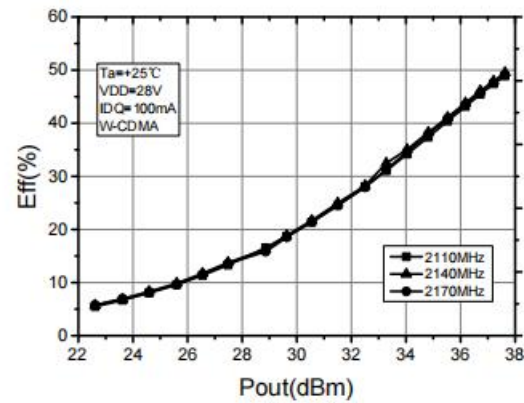


Pulsed CW, Efficiency vs Pout

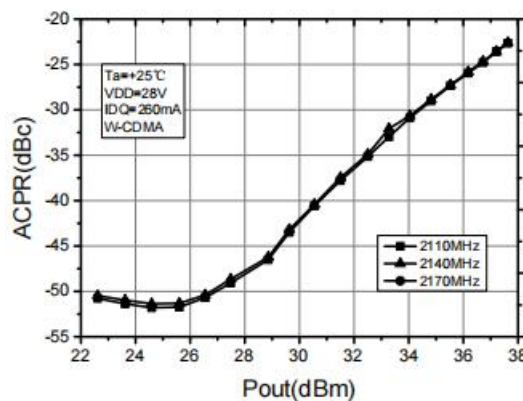
Test conditions unless otherwise noted: 25 °C, VDD = +28Vdc, IDQ= 70mA, PW = 100us, DC= 10% test on HOTLO Application Board



WCDMA, Gain vs Pout



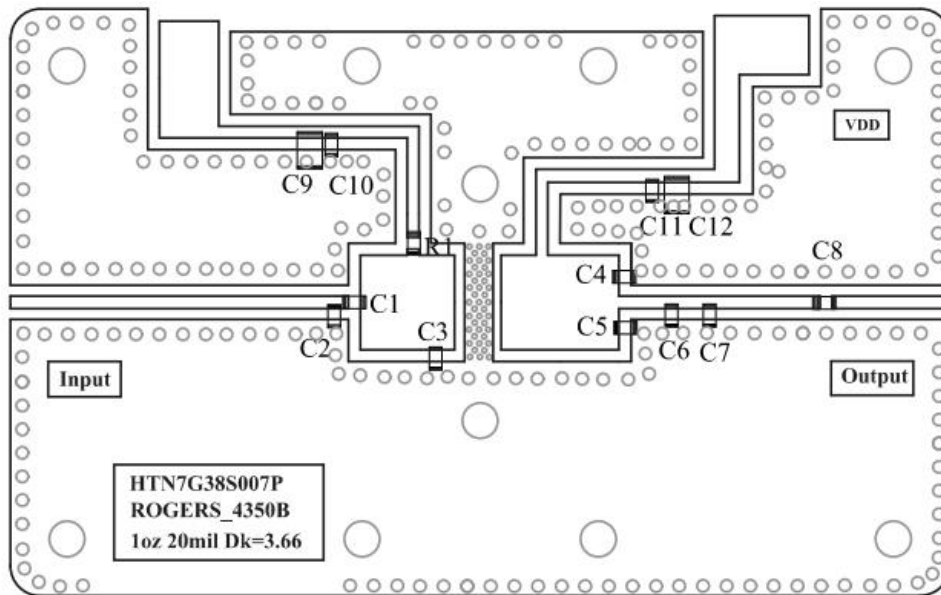
WCDMA, Efficiency vs Pout



WCDMA ACPR_5MHz vs Pout

Test conditions unless otherwise noted: 25 °C, VDD = +28Vdc, IDQ= 70mA, 1C-WCDMA 5MHz Signal, 9.9 dB PAR @ 0.01% CCDF test on HOTLO Application Board

HTN7G38S007P 2620- 2690 MHz Reference Design

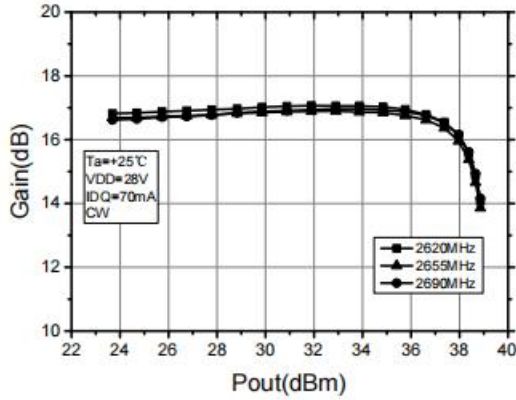


EVB Layout

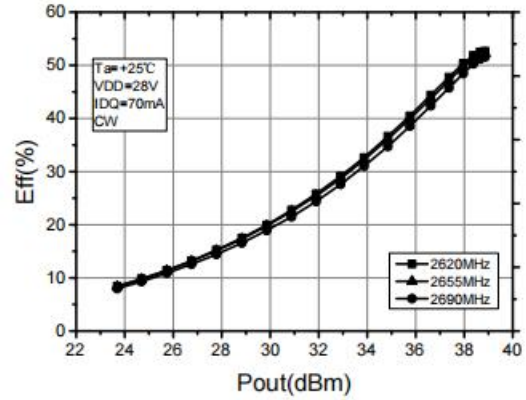
Bill of Materials (BoM) - HTN7G38S007P 2620- 2690 MHz Reference Design

Reference	Value	Description	Manufacturer	P/N
Q1	-	20W, 700 - 3800 MHz LDMOS PA	Holto	HTN7G38S007P
C1	2p2F	MLCC	ATC	600S2R2BT260XT
C2	0p8F	MLCC	ATC	600S0R8BT260XT
C3	0p3F	MLCC	ATC	600S0R3BT260XT
C4	3pF	MLCC	ATC	600S3R0BT260XT
C5	0p5F	MLCC	ATC	600S0R5BT260XT
C6	1p8F	MLCC	ATC	600S1R8BT260XT
C7	0p8F	MLCC	ATC	600S0R8BT260XT
C8, C10, C11	5p6F	MLCC	ATC	600S5R6BT260XT
C9,C12	10uF/50V	MLCC	-	1210
R1	10Ω/0603	Thick Film Resistor	-	-
PCB	Rogers4350B (er = 3.66), 20 mil (0.508 mm), 35 μm (1oz)			

Performance Plots 2620- 2690 MHz Reference Design

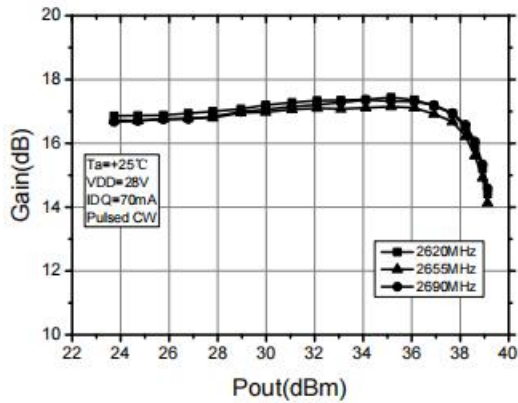


CW, Gain vs Pout

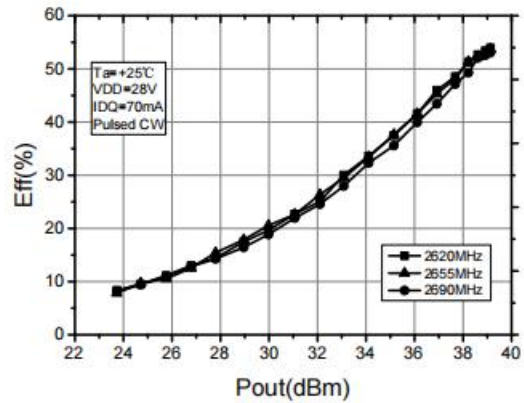


CW, Efficiency vs Pout

Test conditions unless otherwise noted: 25 °C, VDD = +28Vdc, IDQ=70mA test on HOTLO Application Board

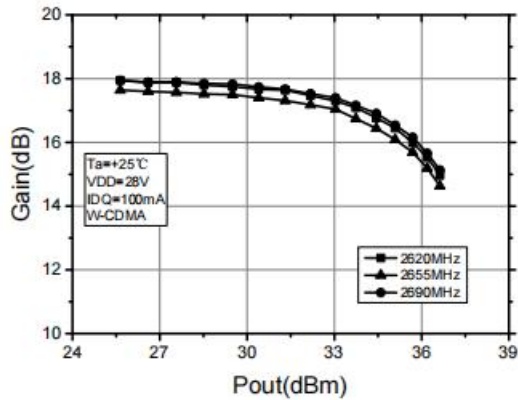


Pulsed CW, Gain vs Pout

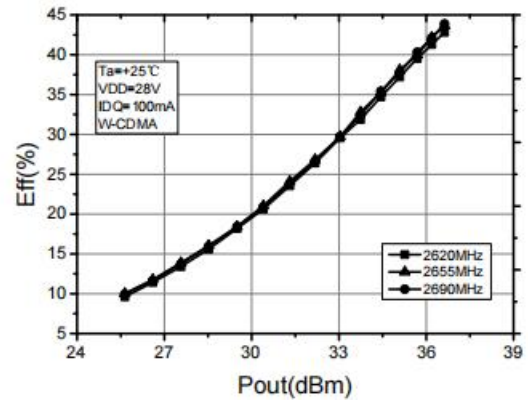


Pulsed CW, Efficiency vs Pout

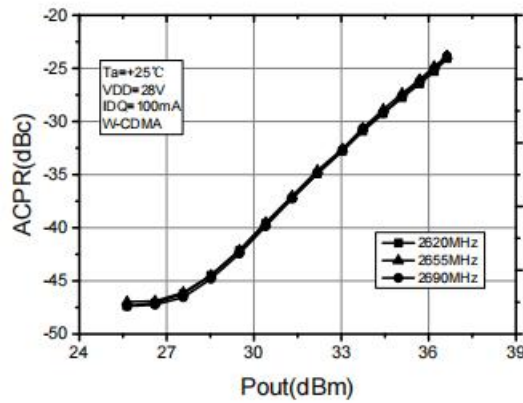
Test conditions unless otherwise noted: 25 °C, VDD = +28Vdc, IDQ= 70mA, PW = 100us, DC= 10% test on HOTLO Application Board



WCDMA, Gain vs Pout



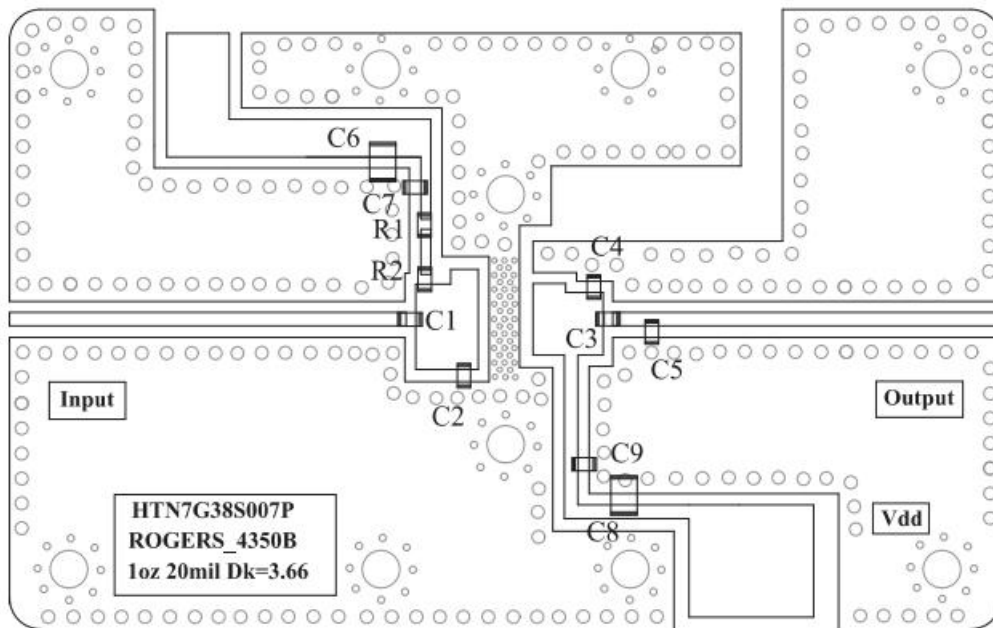
WCDMA, Efficiency vs Pout



WCDMA ACPR_5MHz vs Pout

Test conditions unless otherwise noted: 25 °C, VDD = +28Vdc, IDQ= 70mA, 1C-WCDMA 5MHz Signal, 9.9 dB PAR @ 0.01% CCDF test on HOTLO Application Board

HTN7G38S007P 3300- 3400 MHz Reference Design

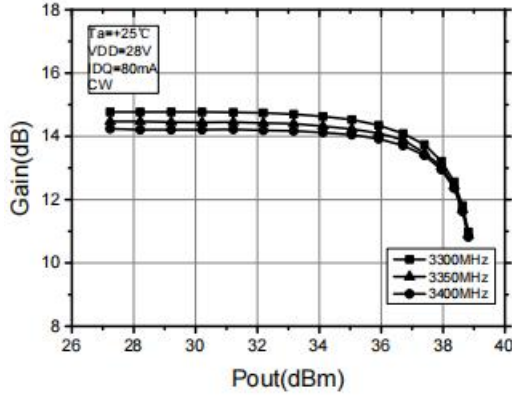


EVB Layout

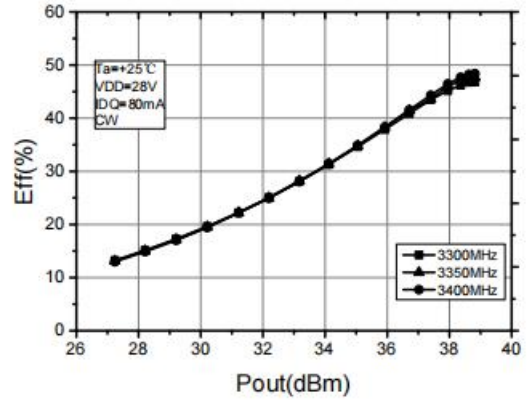
Bill of Materials (BoM) - HTN7G38S007P 3300- 3400 MHz Reference Design

Reference	Value	Description	Manufacturer	P/N
Q1	-	20W, 700 - 3800 MHz LDMOS PA	Holto	HTN7G38S007P
C1, C3, C7, C9	0p3F	MLCC	ATC	600S0R3BT260XT
C2, C5	8p2F	MLCC	ATC	600S8R2BT260XT
C4	1pF	MLCC	ATC	600S1R0BT260XT
C6, C8	10uF/50V	MLCC	-	1210
R1, R2	4.7Ω/0603	Thick Film Resistor	-	-
PCB	Rogers4350B (er = 3.66), 20 mil (0.508 mm), 35 μm (1oz)			

Performance Plots 3300- 3400 MHz Reference Design

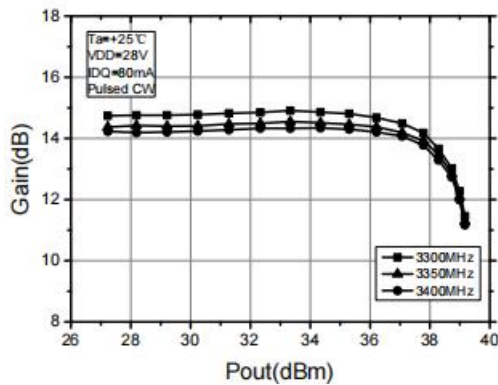


CW, Gain vs Pout

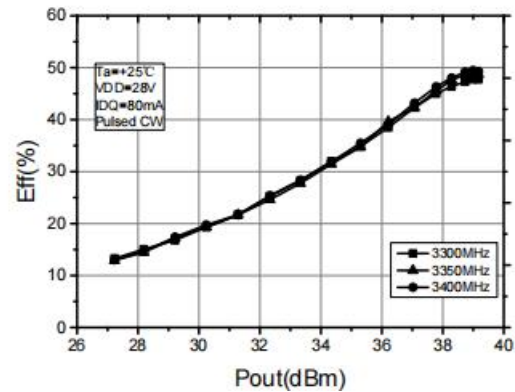


CW, Efficiency vs Pout

Test conditions unless otherwise noted: 25°C , $V_{DD} = +28\text{Vdc}$, $I_{DQ} = 70\text{mA}$ test on HOTLO Application Board

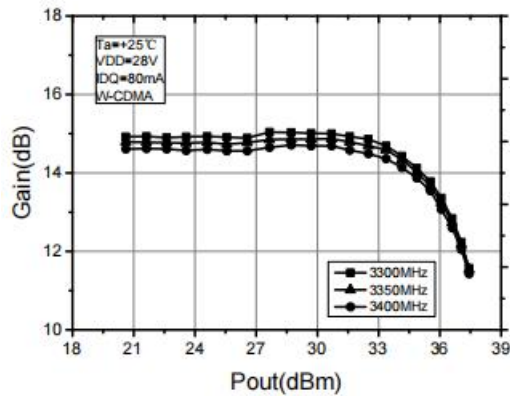


Pulsed CW, Gain vs Pout

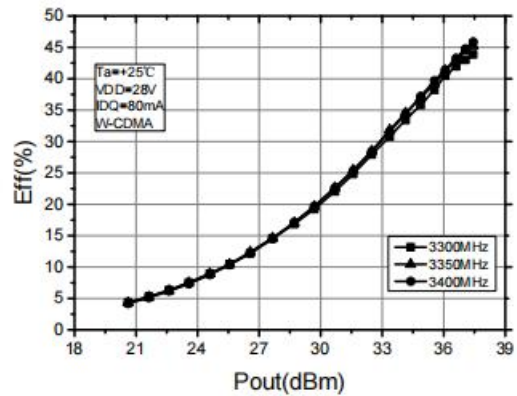


Pulsed CW, Efficiency vs Pout

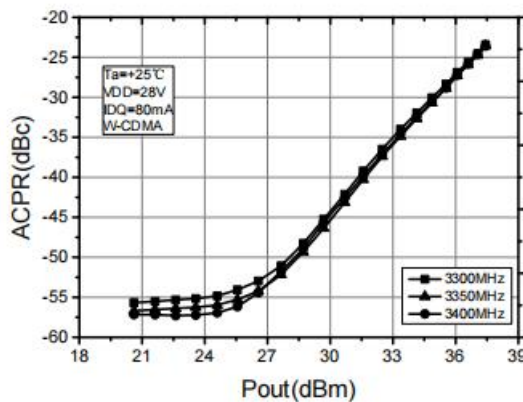
Test conditions unless otherwise noted: 25°C , $V_{DD} = +28\text{Vdc}$, $I_{DQ} = 70\text{mA}$, $PW = 100\mu\text{s}$, $DC = 10\%$ test on HOTLO Application Board



WCDMA, Gain vs Pout



WCDMA, Efficiency vs Pout



WCDMA ACPR_5MHz vs Pout

Test conditions unless otherwise noted: 25 °C, VDD = +28Vdc, IDQ= 70mA, 1C-WCDMA 5MHz Signal, 9.9 dB PAR @ 0.01% CCDF test on HOTLO Application Board

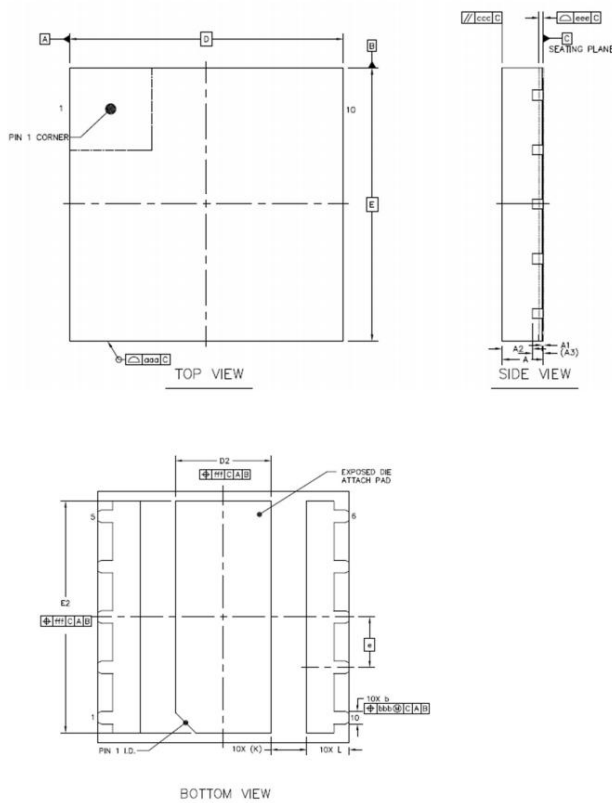
Package Marking and Dimensions



- Line1 (fixed): Device name in W/O
- Line2 (unfixed): Marking Lot No in W/O (Sample: E596-20140001)
- Line3 (unfixed): Date Code + JY

This Marking SPEC only stipulates the content of Marking. For marking requirements such as font and size, please refer to the latest version of "Holto Product Printing Specification"

Marking

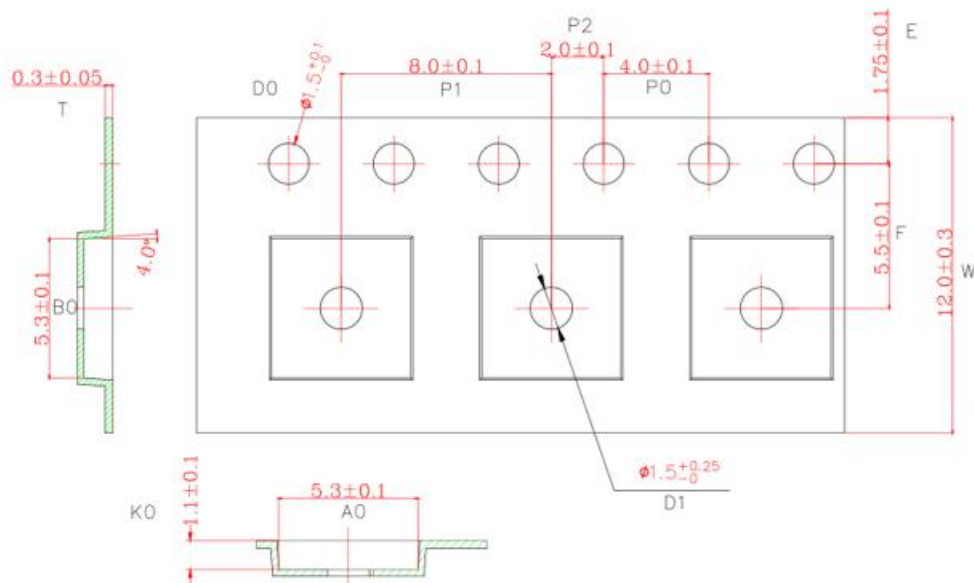


	SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS	A	0.7	0.75	0.8
STAND OFF	A1	0	0.02	0.05
MOLD THICKNESS	A2	---	0.55	---
L/F THICKNESS	A3	0.203 REF		
LEAD WIDTH	b	0.2	0.25	0.3
BODY SIZE	X	D		
	Y	E		
LEAD PITCH	e	1 BSC		
EP SIZE	X	D2	1.8	1.9
	Y	E2	4.5	4.6
LEAD LENGTH	L	0.75	0.85	0.95
LEAD TIP TO EXPOSED PAD EDGE	K	0.7 REF		
PACKAGE EDGE TOLERANCE	aaa	0.1		
MOLD FLATNESS	ccc	0.1		
COPLANARITY	eee	0.08		
LEAD OFFSET	bbb	0.1		
EXPOSED PAD OFFSET	fff	0.1		

Package Dimensions

Tape and Reel Information


Package Type	Reel Size(inch)	Qty/Reel(pcs)	Qty/Box(pcs)	Qty/Carton(pcs)
PDFN5X5	7inch	1000	8000	32000



Tape & Reel Packaging Descriptions

Handling Precautions

Parameter	Grade
Moisture Sensitivity Level MSL	3

Parameter	Rating	Standard	
ESD – Human Body Model (HBM)	Class 1B	JESD22-A114	
ESD – Human Body Model (MM)	Class A	EIA/JESD22-A115	
ESD – Charged Device Model (CDM)	Class III	JESD22-C101	

RoHS Compliance

This product is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU.

Datasheet Status

Document status	Product status	Definition
Objective Datasheet	Design simulation	Product objective specification
Preliminary Datasheet	Customer sample	Engineering samples and first test results
Product Datasheet	Mass production	Final product specification

Abbreviations

Acronym	Definition
LDMOS	Laterally-Diffused Metal-Oxide Semiconductor
CW	Continuous Waveform

Revision history

Document ID	Datasheet Status	Release Date	Revision Version
Rev 2.4	Product	April 2021	Corrected the operating junction temperature
Rev 2.5	Product	March 2023	New format based on English version datasheet
Rev 2.6	Product	April 2024	Update TBD information

Contact Information

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