HTN7G09S060P

60W, 1.8 - 1000 MHz LDMOS Amplifier

Product datasheet

Description

The HTN7G09S060P is an unmatched discrete LDMOS Power Amplifier with 60W saturated output power covering frequency range from 1.8 - 1000 MHz.

Features

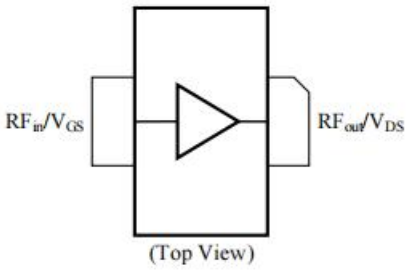
- Operating Frequency Range: 1.8 - 1000 MHz
- Operating Drain Voltage: +28V
- Saturation Output Power: 60W
- Power Average: 8W
- Excellent thermal stability due to low thermal resistance package
- Enhanced robustness design without device degradation
- Internally integrated enhanced ESD design

Applications

- CDMA
- W-CDMA
- GSM EDGE
- MC-GSM
- TDD/FDD LTE
- WiMAX
- ISM

TO-270

Over-Molded 2 leads (Straight)



Note: Exposed backside of the package is the source terminal for the transistor

Pin Connections

Ordering Information

Part Number	Description
HTN7G09S060P	Reel Package
HTN7G09S060P EVB	700 - 960 MHz EVB

Typical Performance

RF Characteristics (WCDMA)

Freq (MHz)	Gain (dB)	Eff (%)	ACPR_L* @5MHz (dBc)	IRL (dB)
920	22.1	19.0	-45.3	10
940	21.8	19.5	-46.3	12
960	21.0	20.7	-47.8	8

Test conditions unless otherwise noted: 25 °C, VDD = +28Vdc, IDQ= 550mA, P_{AVG} = 39 dBm (7.94W), 1C-WCDMA 5MHz Signal, 9.9 dB PAR @ 0.01% CCDF test on HOTLO Application Board

**Uncorrected DPD*

Absolute Maximum Ratings

Parameter	Range/Value	Unit
Drain voltage (V_{DSS})	-0.5, +65	V
Gate voltage (V_{GS})	-5 to +10	V
Operation voltage (V_{DD})	+0 to +28	V
Storage Temperature (T_{STG})	-55 to +150	°C
CasecTemperature (T_C)	-40 to +150	°C
Junction Temperature (T_J)	-40 to +225	°C

Electrical Specification

DC Characteristics

Parameter	Conditions	Min	Typ	Max	Unit
Breakdown Voltage $V_{(BR)DSS}$	Vgs=0V, Ids=48uA	65	-	-	V
Gate-Source Threshold Voltage $V_{GS(th)}$	Vds=Vgs, Ids=48uA	0.8	1.3	1.8	V
Drain Leakage Current I_{DSS}	Vgs=0V, Vds=65V	-	-	10	uA
Gate Leakage Current I_{GSS}	Vgs=5V, Vds=0V	-	-	1	uA

Load Mismatch Test

Condition	Test Result
VSWR=10:1, at all Phase Angles, VDD = +28Vdc, IDQ= 400mA, CW signal 100W @940 MHz test on HOTLO Application Board	No Device Degradation

Thermal Information

Parameter	Condition	Value (Typ)	Unit
Thermal Resistance Junction to Case (R_{TH})	T_{CASE}= 60°C, VDD = +28Vdc, IDQ= 400mA, CW signal 60W	0.95	°C /W

Load Pull Performance for Maximum Power (P1dB/P3dB)

Test conditions unless otherwise noted: 25 °C, VDD = +28Vdc, IDQ= 400mA, PW = 40us, DC= 4%

Max Output Power P1dB						
Freq (MHz)	Z_source (Ω)	Z_load [1] (Ω)	Gain (dB)	P1dB (dBm)	P1dB (W)	Eff (%)
920	0.78-j*0.90	2.22-j*0.20	22.0	49.87	**97.05**	56.92
1400	0.74-j*3.05	1.59-j*0.93	19.27	49.67	**92.68**	58.91
1800	0.34-j*3.35	1.33-j*2.96	16.70	48.96	**78.70**	52.68

[1] Load impedance for optimum P1dB pout

Max Output Power P3dB						
Freq (MHz)	Z_source (Ω)	Z_load [2] (Ω)	Gain (dB)	P3dB (dBm)	P3dB (W)	Eff (%)
920	0.78-j*0.90	2.26-j*0.65	22.02	50.89	**122.74**	61.81
1400	0.74-j*3.05	1.66-j*1.29	18.89	50.77	**119.40**	60.61
1800	0.34-j*3.35	1.57-*j3.12	16.68	50.13	**103.04**	55.67

[2] Load impedance for optimum P3dB pout

Load Pull Performance for Maximum Efficiency (P1dB/P3dB)

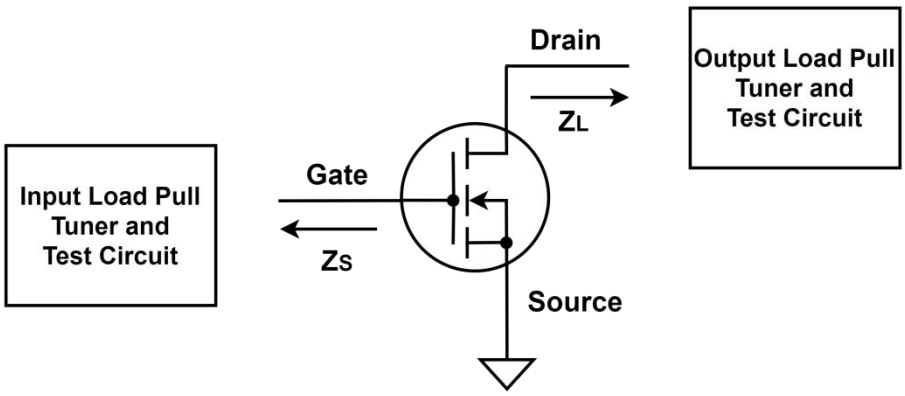
Test conditions unless otherwise noted: 25 °C, VDD = +28Vdc, IDQ= 400mA, PW = 40us, DC= 4%

Max Efficiency P1dB						
Freq (MHz)	**Z_source (Ω)**	**Z_load [1] (Ω)**	**Gain (dB)**	**P1dB (dBm)**	**P1dB (W)**	**Eff (%)**
920	0.78-j*0.90	2.56+j*1.75	24.74	48.22	66.37	**72.51**
1400	0.74-j*3.05	1.54+j*0.34	21.48	47.57	57.15	**69.45**
1800	0.34-j*3.35	1.08-j*2.06	18.96	47.57	57.15	**59.14**

[1] Load impedance for optimum P1dB efficiency

Max Efficiency P3dB						
Freq (MHz)	**Z_source (Ω)**	**Z_load [2] (Ω)**	**Gain (dB)**	**P3dB (dBm)**	**P3dB (W)**	**Eff (%)**
920	0.78-j*0.90	2.31+j*1.06	24.70	49.24	83.95	**76.91**
1400	0.74-j*3.05	1.61+j*0.04	21.00	49.33	85.70	**71.75**
1800	0.34-j*3.35	1.29-j*2.37	18.19	49.32	85.51	**61.43**

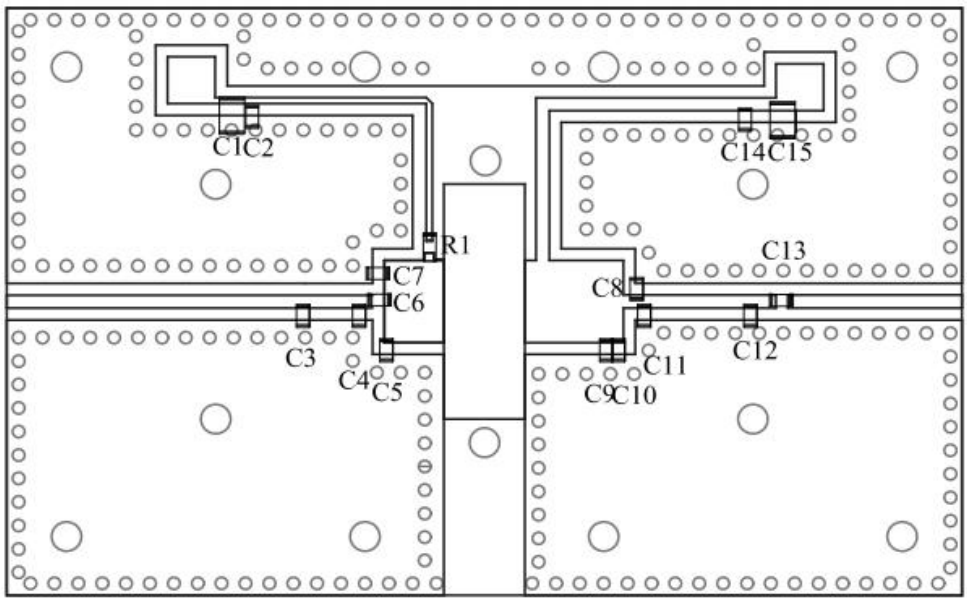
[2] Load impedance for optimum P3dB efficiency



Z_source : Measured impedance presented to the input of the device at the package reference plane

Z_load : Measured impedance presented to the output of the device at the package reference plane

HTN7G09S060P 920 - 960 MHz Reference Design

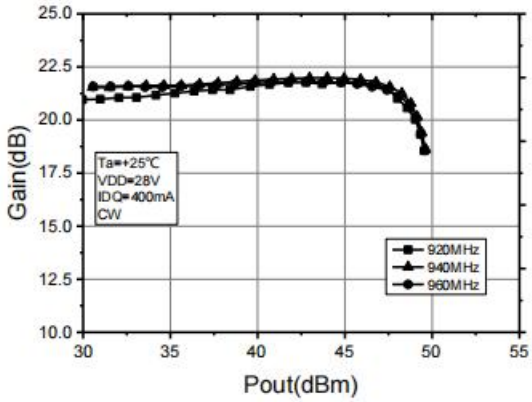


EVB Layout

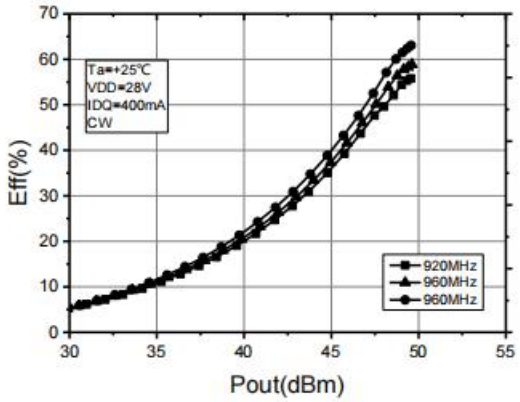
Bill of Materials (BoM) - HTN7G09S060P 920 - 960 MHz Reference Design

Reference	Value	Description	Manufacturer	P/N
Q1	-	60W, 1.8 - 1000 MHz LDMOS PA	Holto	HTN7G09S060P
C2, C6, C13, C14	47pF	MLCC	ATC	600S470BT260XT
C3, C4, C5, C7, C8	8.2pF	MLCC	ATC	600S8R2BT260XT
C11, C12	4.3pF	MLCC	ATC	600S4R3BT260XT
C9	2.5pF	MLCC	ATC	600S2R5BT260XT
C10	2pF	MLCC	ATC	600S2R0BT260XT
C15	10uF	MLCC	Murata	GRM32EC72A106KE05
C1	4.7uF	MLCC	Murata	GRM31CR71H475KA12L
R1	10Ω	Thick Film Resistor	YAGEO	RC0603FR-0710RL
PCB	Rogers4350B (er = 3.66), 30 mil (0.762 mm), 35 µm (1oz)			

Performance Plots

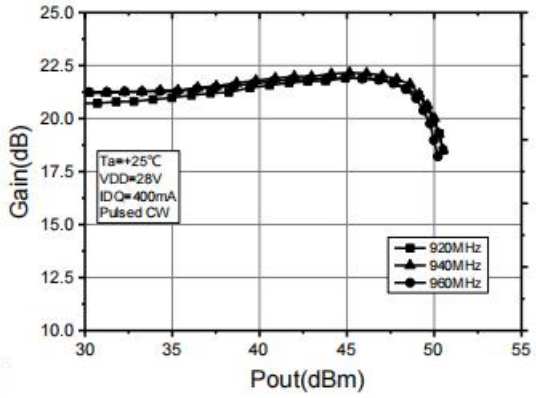


CW, Gain vs Pin

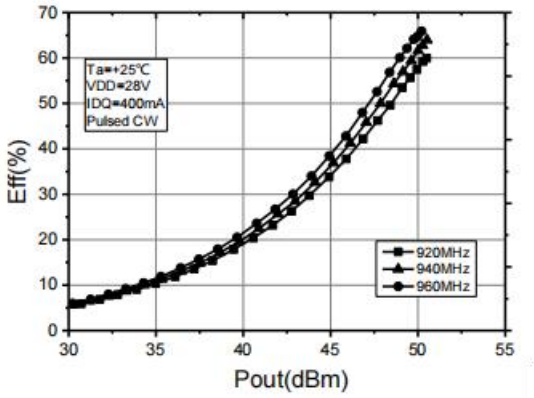


CW, Efficiency vs Pout

Test conditions unless otherwise noted: 25 °C, VDD = +28Vdc, IDQ=400mA test on HOTLO Application Board

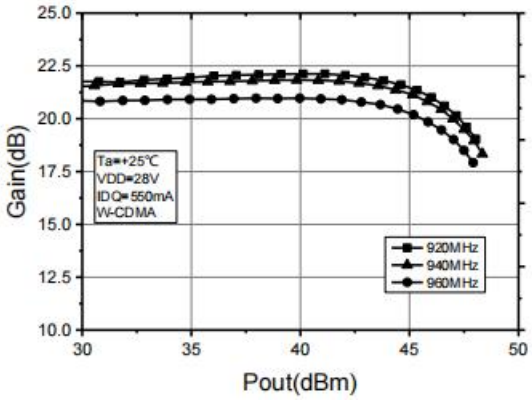


Pulsed CW, Pout vs Pin

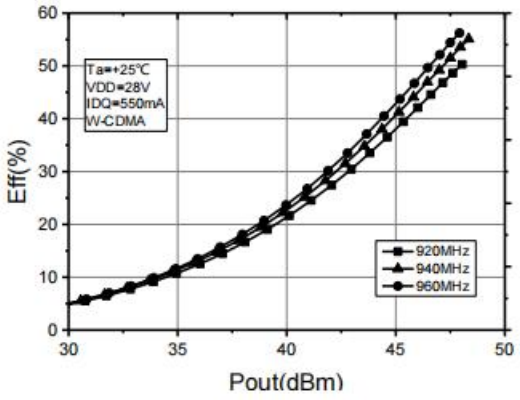


Pulsed CW, Efficiency vs Pout

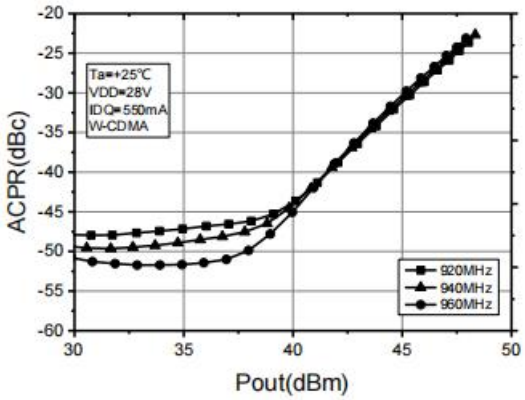
Test conditions unless otherwise noted: 25 °C, VDD = +28Vdc, IDQ=400mA, PW = 100us, DC= 10% test on HOTLO Application Board



WCDMA, Gain vs Pout

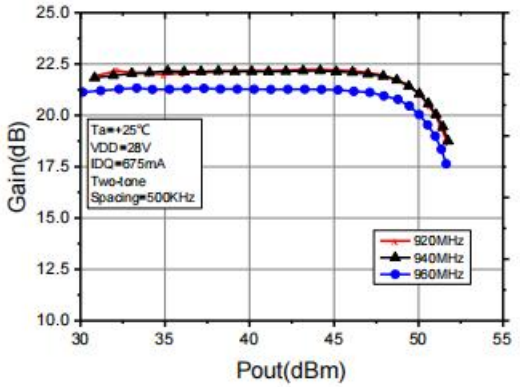


WCDMA, Efficiency vs Pout

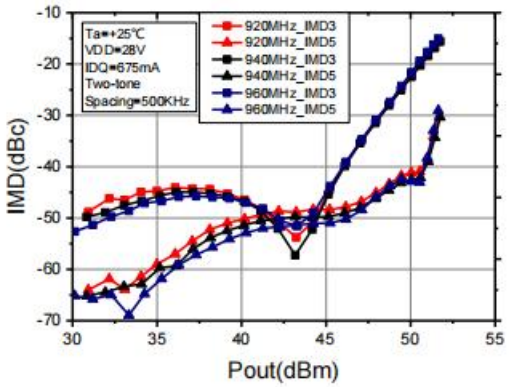


WCDMA, ACPR_5MHz, ACPR_10MHz vs Pout

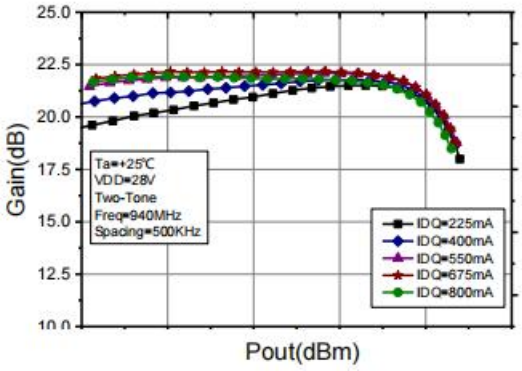
Test conditions unless otherwise noted: 25 °C, VDD = +28Vdc, IDQ=550mA, 1C-WCDMA 5MHz Signal, 9.9 dB PAR @ 0.01% CCDF test on HOTLO Application Board



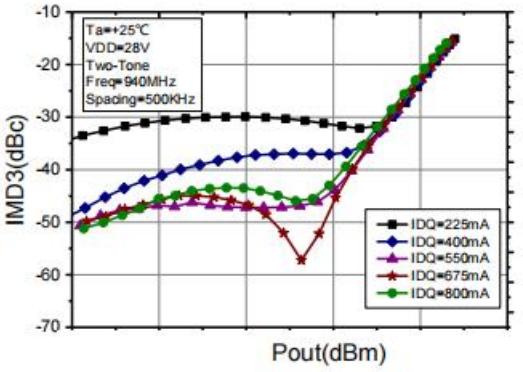
Two Tones Gain vs Pout (PEP) @Freq's



Two Tones IMD vs Pout (PEP) @Freq's



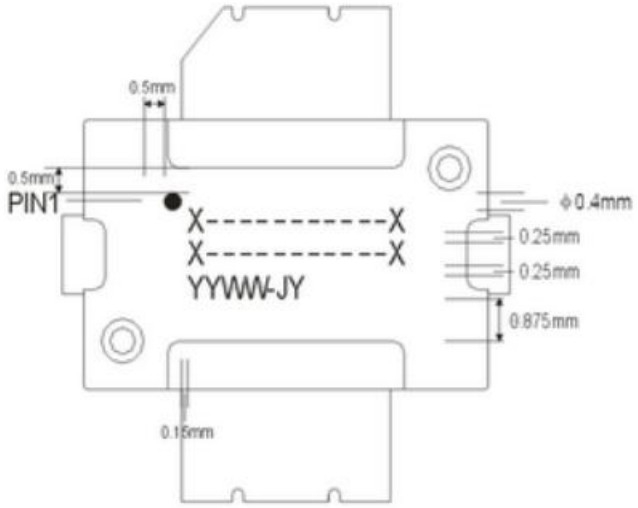
Two Tones Gain vs Pout (PEP) @Idq's



Two Tones IMD vs Pout (PEP) @Idq's

Test conditions unless otherwise noted: 25 °C, VDD = +28Vdc, IDQ=675mA, Two tone Test, Carrier Spacing @500KHz test on HOTLO Application Board

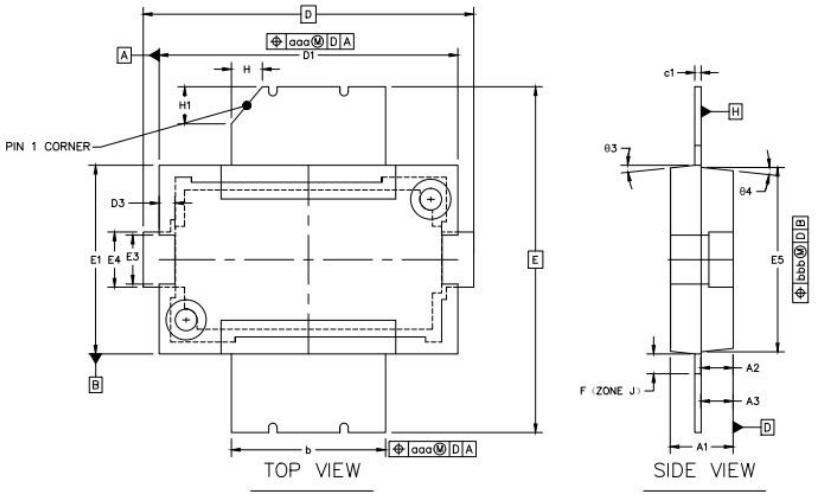
Package Marking and Dimensions

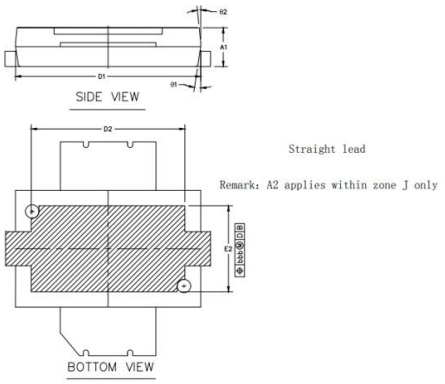


- Line1 (fixed): Device name in W/O
- Line2 (unfixed): Marking Lot No in W/O
(Sample: E596-20140001)
- Line3 (unfixed): Date Code + JY

This Marking SPEC only stipulates the content of Marking. For marking requirements such as font and size, please refer to the latest version of “Holto Product Printing Specification”

Marking



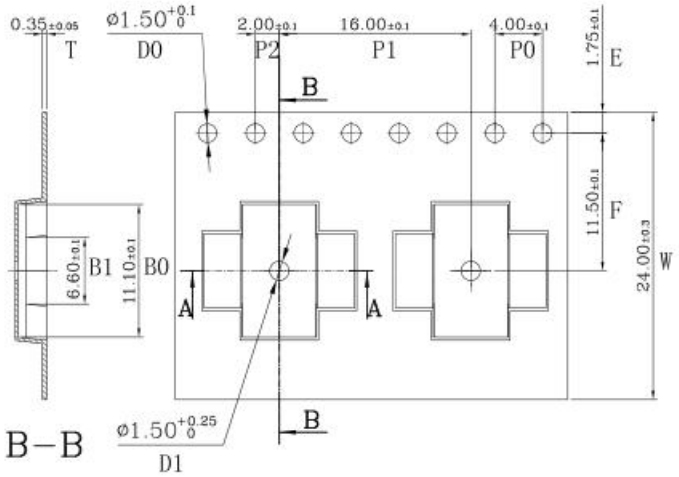


		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A1	1.98	2.03	2.08
MOLD THICKNESS		A2	1.02	1.045	1.07
		A3	0.99	1.04	1.09
L/F THICKNESS		C1		0.203 REF	
BODY SIZE	X	D	10.57	10.67	10.77
	Y	E	11.08	11.18	11.28
CION SIZE	X	D2		7.37 MIN	
	Y	E2		3.81 MIN	
MOLD LENGTH		D1	9.6	9.65	9.7
LENGTH		D3	0.41	0.51	0.61
MOLD WIDTH		E1	6.05	6.1	6.15
WIDTH		E3	1.48	1.58	1.68
		E4	1.68	1.78	1.88
		E5	5.91	5.96	6.01
ZONE WIDTH		F		0.64 BSC	
LEAD WIDTH		b	4.9	4.98	5.06
PACKAGE EDGE TOLERANCE		aaa		0.1	
LEAD OFFSET		bbb		0.2	
TAPER ANGLE		θ1	7°	9°	11°
		θ2	4°	6°	8°
		θ3	4°	6°	8°
		θ4	4°	6°	8°
PIN1 SIZE		H		1 REF	
		H1		1.2 REF	

Package Dimensions

Tape and Reel Information

Package Type	Reel Size(inch)	Qty/Reel(pcs)	Qty/Box(pcs)	Qty/Carton(pcs)
TO270	13inch	1500	1500	7500



Tape & Reel Packaging Descriptions

Handling Precautions

Parameter	Grade
Moisture Sensitivity Level MSL	3

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 1B	JESD22-A114
ESD – Human Body Model (MM)	Class A	EIA/JESD22-A115
ESD – Charged Device Model (CDM)	Class III	JESD22-C101

RoHS Compliance

This product is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU.

Datasheet Status

Document status	Product status	Definition
Objective Datasheet	Design simulation	Product objective specification
Preliminary Datasheet	Customer sample	Engineering samples and first test results
Product Datasheet	Mass production	Final product specification

Abbreviations

Acronym	Definition
LDMOS	Laterally-Diffused Metal-Oxide Semiconductor
CW	Continuous Waveform

Revision history

Document ID	Datasheet Status	Release Date	Revision Version
Rev 2.2	Product	March 2023	New format based on English version datasheet
Rev 2.3	Product	March 2024	Version released after re review
Rev 2.4	Product	June 2024	Update package 3D picture

Contact Information

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