# HTH9G09P700S

## 700W, 700 - 960 MHz LDMOS Amplifier

Product datasheet

## Description

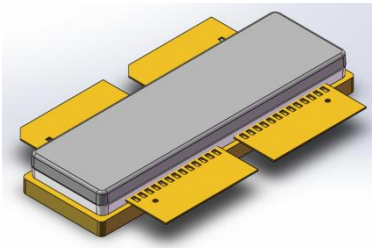
The HTH9G09P700S is an unmatched discrete LDMOS Power Amplifier with 700W saturated output power covering frequency range from 700 - 960 MHz.

## Features

- Operating Frequency Range: 700 - 960 MHz
- Operating Drain Voltage: +48V
- Saturation Output Power: 700W
- Power Average: 100W
- Device can be used on a single-ended or in a push-pull configuration. Doherty application applicable
- Excellent thermal stability due to low thermal resistance package
- Enhanced robustness design without device degradation
- Efficiency: 54%@758MHz, WCDMA
- Gain: 19.5dB@758MHz, WCDMA

## Applications

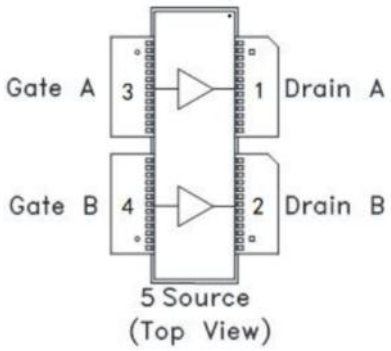
- 3GPP 5G NR FR1 n5/8/12/13/14/18/20/26/28/29/67/85/100
- 4G-LTE B5/8/12/13/14/17/18/19/20/26/28/67/85/103
- Amplifier for Micro and Macro Base Stations
- Repeaters/DAS
- Mobile Infrastructure



**ACS3210-4L**

RoHS compliant

Air Cavity Splice
Earless Flanged balanced Ceramic Package;
4 Leads




Note: Exposed backside of the package is the source terminal for the transistor

**Pin Connections**

## Ordering Information

| Part Number | Description |
|---|---|
| HTH9G09P700S | Reel Package |
| HTH9G09P700SEVB | 758- 803 MHz EVB |

## Typical Performance

### RF Characteristics (Pulsed CW)

| Freq (MHz) | P5dB (dBm) | Gain (dB) | Eff (%) | IRL (dB) |
|---|---|---|---|---|
| 758 | 59.3 | 20.2 | 53 | 10 |
| 780.5 | 59.2 | 20.5 | 53 | 12 |
| 803 | 59.2 | 19.9 | 57 | 15 |

*Test conditions unless otherwise noted: 25 °C, VDD = +48Vdc, IDQ_Carrier= 450mA, Vgsp = Vgsc - 1.7V, PW = 100us, DC= 10% test on HOTLO Application Board*

### RF Characteristics (WCDMA)

| Freq (MHz) | Gain (dB) | Eff (%) | ACPR* @5MHz (dBc) | ACPR* @10MHz (dBc) | IRL (dB) |
|---|---|---|---|---|---|
| 758 | 19.5 | 54.0 | -24.2 | -24.2 | 10 |
| 780.5 | 19.5 | 54.9 | -25.0 | -25.0 | 13 |
| 803 | 19.1 | 54.5 | -26.9 | -26.9 | 15 |

*Test conditions unless otherwise noted: 25 °C, VVDD = +48Vdc, IDQ_Carrier= 450mA, Vgsp = Vgsc - 1.7V, $P_{AVG}$ = 49 dBm 1C-WCDMA 5MHz Signal, 9.9 dB PAR @ 0.01% CCDF test on HOTLO Application Board*

**Uncorrected DPD*

## Absolute Maximum Ratings

| Parameter | Range/Value | Unit |
|---|---|---|
| Drain voltage ($V_{DSS}$) | -0.5 to +110 | V |
| Gate voltage ($V_{GS}$) | -5 to +10 | V |
| Storage Temperature ($T_{STG}$) | -55 to +150 | °C |
| Junction Temperature ($T_J$) | -40 to +225 | °C |

## Electrical Specification

### DC Characteristics (Carrier)

| Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Breakdown Voltage $V_{(BR)DSS}$ | Vgs=0V, Ids=180uA | 110 | - | - | V |
| Gate-Source Threshold Voltage $V_{GS(th)}$ | Vgs=10V, Ids=180uA | - | 2.7 | - | V |
| Drain Leakage Current $I_{DSS}$ | Vgs=0V, Vds=110V | - | - | 500 | nA |
| Gate Leakage Current $I_{GSS}$ | Vgs=10V, Vds=0V | - | - | 500 | nA |

### DC Characteristics (Peak)

| Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Breakdown Voltage $V_{(BR)DSS}$ | Vgs=0V, Ids=360uA | 110 | - | - | V |
| Gate-Source Threshold Voltage $V_{GS(th)}$ | Vgs=10V, Ids=360uA | - | 2.7 | - | V |
| Drain Leakage Current $I_{DSS}$ | Vgs=0V, Vds=110V | - | - | 500 | nA |
| Gate Leakage Current $I_{GSS}$ | Vgs=10V, Vds=0V | - | - | 500 | nA |

### Load Mismatch Test

| Condition | Test Result |
|---|---|
| VSWR=10:1, at all Phase Angles, VDD = +48Vdc, IDQ_Carrier= 450mA, Vgsp = Vgsc - 1.7V, 1C-WCDMA 5MHz Signal, 9.9 dB PAR, $P_{AVG}$ = 52 dBm, Frequency 780.5 MHz test on HOTLO Application Board | No Device Degradation |

### Thermal Information

| Parameter | Condition | Value (Typ) | Unit |
|---|---|---|---|
| Thermal Resistance Junction to Case ($R_{TH}$) | $T_{CASE}$= 80°C, VDD = +48Vdc, IDQ_Carrier= 450mA, Vgsp = Vgsc - 1.7V, 1C-WCDMA 5MHz Signal, 9.9 dB PAR, $P_{AVG}$ = 53 dBm | 0.46 | °C /W |

## Load Pull Performance Carrier

*Test conditions unless otherwise noted: 25 °C, VDD = +48Vdc, IDQ= 450mA, PW = 100us, DC= 10%*

| Max Output Power (Carrier) | | | | | | |
|---|---|---|---|---|---|---|
| **Freq (MHz)** | **Z_source (Ω)** | **Z_load [1] (Ω)** | **Gain (dB)** | **P3dB (dBm)** | **P3dB (W)** | **Eff (%)** |
| 760 | 3.5-j*1.5 | 1.9+j*0.2 | 22.6 | 55.5 | 360 | 69.0 |
| 860 | 3.8-j*4.7 | 1.7+j*0.12 | 21.7 | 55.4 | 350 | 68.0 |
| 960 | 7.3-j*8.9 | 1.5-j*0.4 | 20.5 | 55.3 | 340 | 63.0 |

*[1] Load impedance for optimum P3dB pout*

| Max Drain Efficiency (Carrier) | | | | | | |
|---|---|---|---|---|---|---|
| **Freq (MHz)** | **Z_source (Ω)** | **Z_load [2] (Ω)** | **Gain (dB)** | **P3dB (dBm)** | **P3dB (W)** | **Eff (%)** |
| 760 | 3.5-j*1.5 | 1.5+j*1.7 | 24.5 | 53.6 | 230 | 77.0 |
| 860 | 3.8-j*4.7 | 1.4+j*1.3 | 23.5 | 53.7 | 235 | 75.0 |
| 960 | 7.3-j*8.9 | 1.3+j*0.8 | 22.3 | 54.0 | 255 | 71.2 |

*[2] Load impedance for optimum P3dB efficiency*

## Load Pull Performance Peak

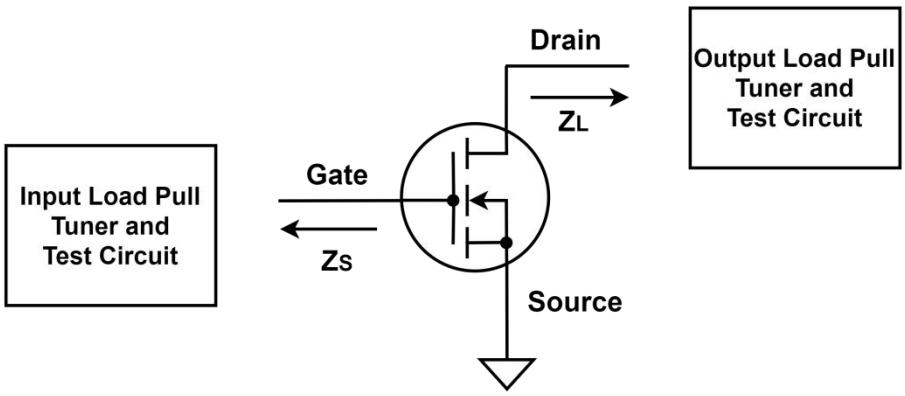
*Test conditions unless otherwise noted: 25 °C, VDD = +48Vdc, IDQ= 700mA, PW = 100us, DC= 10%*

| Max Output Power (Peak) | | | | | | |
|---|---|---|---|---|---|---|
| Freq (MHz) | Z_source (Ω) | Z_load [1] (Ω) | Gain (dB) | P3dB (dBm) | P3dB (W) | Eff (%) |
| 760 | 1.7-j*0.8 | 0.8+j*0.7 | 22.3 | 58.1 | 650 | 65.5 |
| 860 | 1.9-j*2.1 | 0.8+j*0.5 | 21.5 | 58.0 | 640 | 64.0 |
| 960 | 3-j*4.5 | 0.8+j*0.0 | 20.2 | 57.9 | 620 | 61.0 |

*[1] Load impedance for optimum P3dB pout*

| Max Drain Efficiency (Peak) | | | | | | |
|---|---|---|---|---|---|---|
| Freq (MHz) | Z_source (Ω) | Z_load [2] (Ω) | Gain (dB) | P3dB (dBm) | P3dB (W) | Eff (%) |
| 760 | 1.7-j*0.8 | 1.1-j*0.0 | 24.0 | 57.0 | 498 | 75.0 |
| 860 | 1.9-j*2.1 | 0.9-j*0.1 | 23.2 | 56.5 | 455 | 72.0 |
| 960 | 3-j*4.5 | 0.9-j*0.2 | 22.0 | 56.5 | 450 | 69.0 |

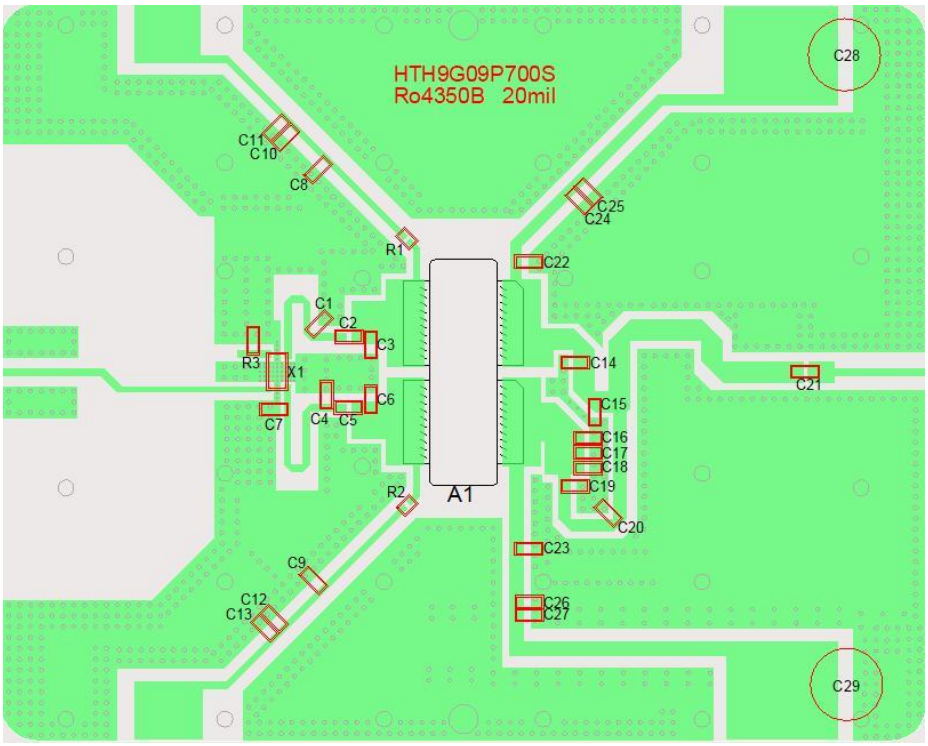
*[2] Load impedance for optimum P3dB efficiency*




*Z_source : Measured impedance presented to the input of the device at the package reference plane*

*Z_load : Measured impedance presented to the output of the device at the package reference plane*

## HTH9G09P700S 925- 960 MHz Reference Design



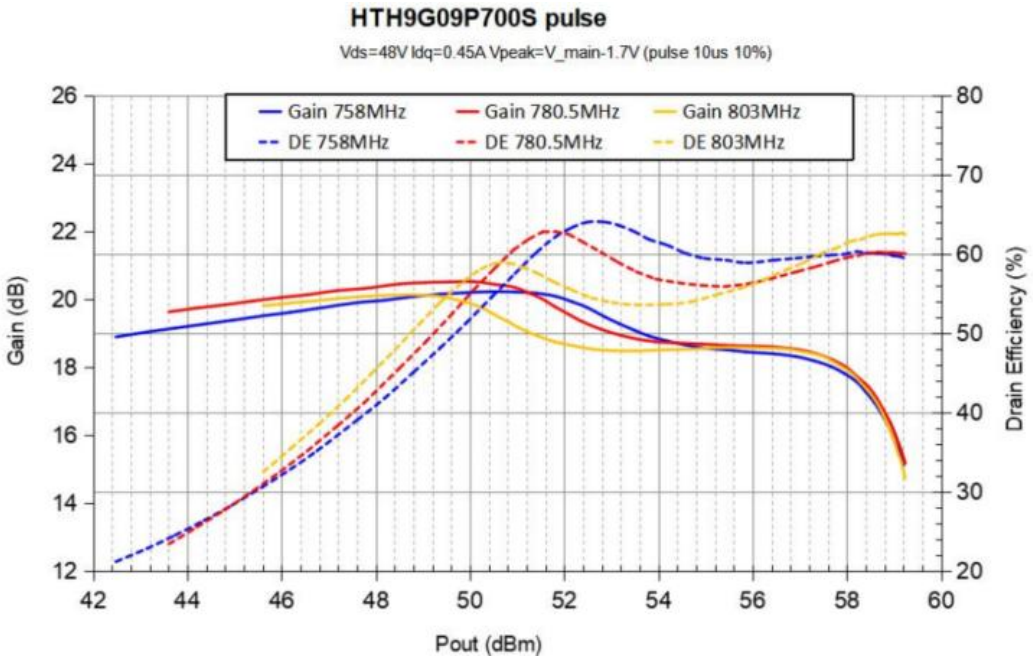

**EVB Layout**

## Bill of Materials (BoM) - HTH9G09P700S 925- 960 MHz Reference Design

| Reference | Value | Description | Manufacturer | P/N |
|---|---|---|---|---|
| Q1 | - | 700W, 700 - 960 MHz LDMOS PA | Holto | HTH9G09P700S |
| C2,C5,C8,C9,C21, C22,C23 | 56pF | MLCC | Murata | GQM2195C2E560JB12 |
| C1,C14 | 12pF | MLCC | Murata | GQM2195C2E120JB12 |
| C3 | 7p5F | MLCC | Murata | GQM2195G2E7R5BB12 |
| C4,C16 | 11pF | MLCC | Murata | GQM2195C2E110JB12 |
| C6 | 15pF | MLCC | Murata | GQM2195C2E150JB12 |
| C7 | 2pF | MLCC | Murata | GQM2195G2E2R0BB12 |
| C15,C19 | 6p2F | MLCC | Murata | GQM2195G2E6R2BB12 |
| C17 | 10pF | MLCC | Murata | GQM2195C2E100JB12 |

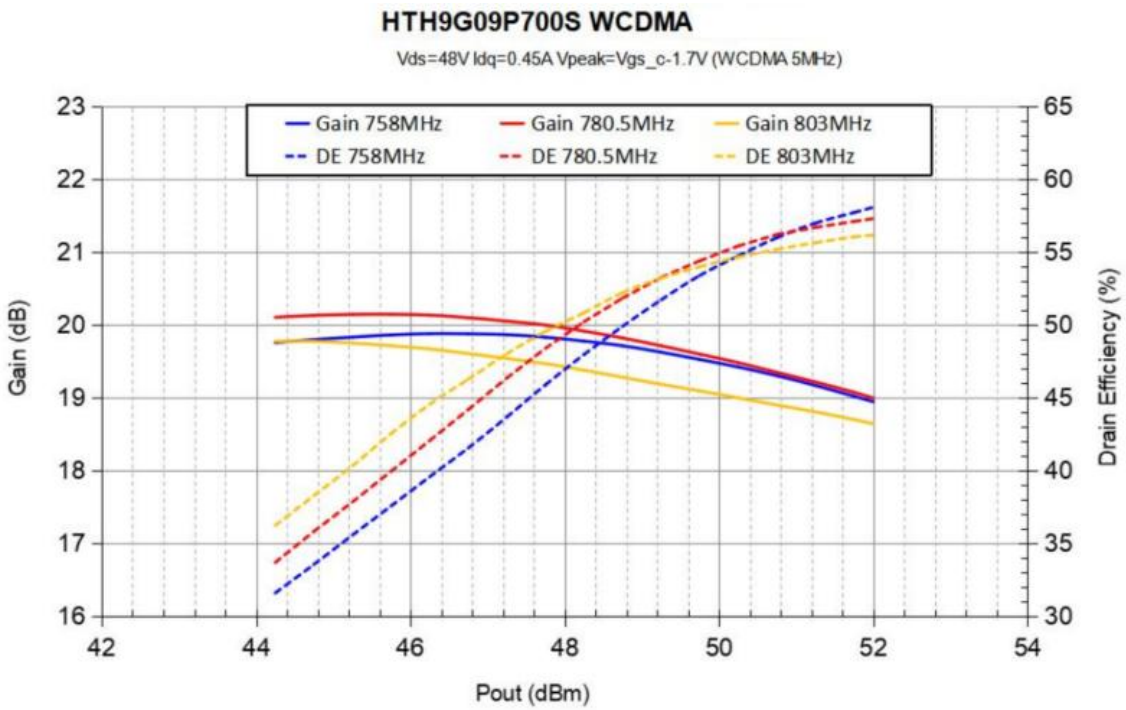
| Reference | Value | Description | Manufacturer | P/N |
|---|---|---|---|---|
| C18 | 9p1F | MLCC | Murata | GQM2195G2E9R1BB12 |
| C20 | 3p9F | MLCC | Murata | GQM2195G2E3R9BB12 |
| C10,C12 | 1uF /100V | MLCC | Murata | GRM32CR72A105KA35 |
| C11,C13 | 4u7F /100V | MLCC | Murata | GRM32DC72A475ME01 |
| C24,C25,C26, C27 | 10uF /100V | MLCC | Murata | GRM32EC72A106KE05 |
| C28,C29 | 220uF /100V | Electrolytic Capacitor | Vishay | MAL213669221E3 |
| R1, R2 | 10Ω | Thick Film Resistor | YAGEO | RC0805FR-0710RL |
| R3 | 50Ω/ 25W | High Frequency/RF Resistors | ANAREN | C16A50Z4 |
| X1 | - | Hybrid Coupler 2dB, 90° | ANAREN | X3C07F1-02S |
| PCB | Rogers 4350B (er = 3.66), 20 mil (0.508 mm), 35 µm (1oz) | | | |

## Performance Plots



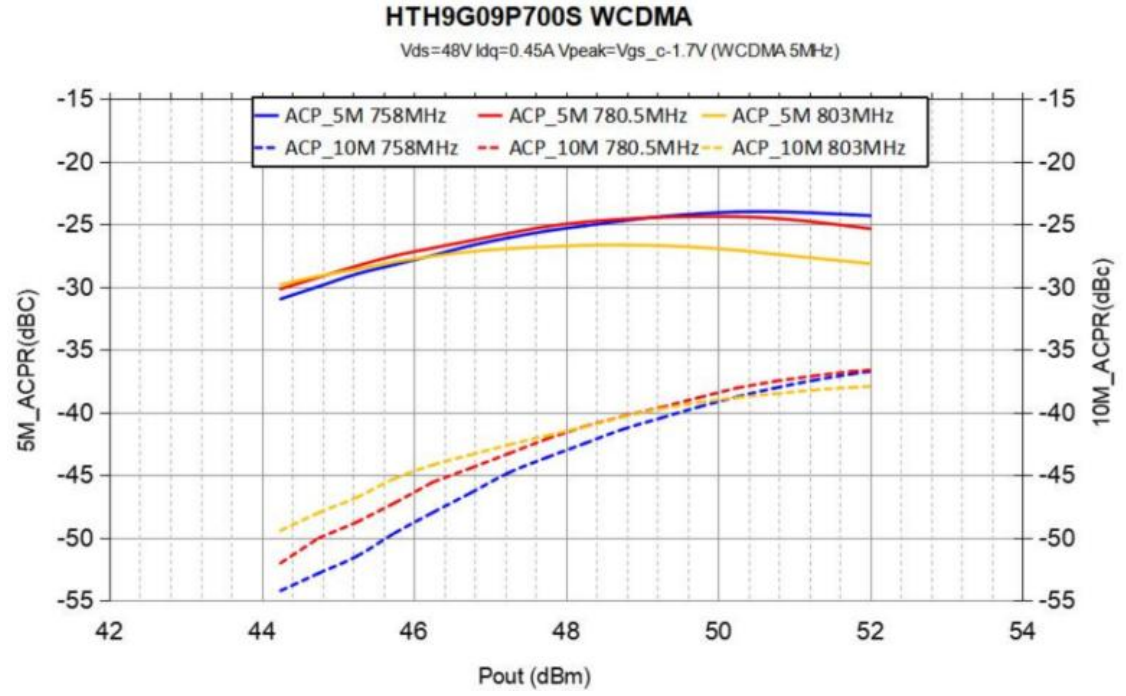

**Pulsed CW, Gain and Efficiency vs Pout**

*Test conditions unless otherwise noted: 25 °C, VDD = +48Vdc, IDQ= 450mA, Vgsp = Vgsc - 1.7V, PW = 100us, DC= 10% test on HOTLO Application Board*




**WCDMA, Gain and Efficiency vs Pout**

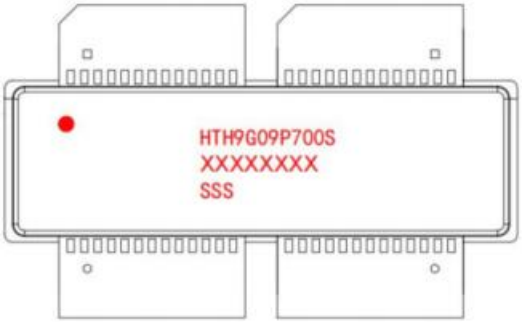
*Test conditions unless otherwise noted: 25 °C, VDD = +48Vdc, IDQ = 450mA, Vgsp = Vgsc - 1.7V, 1C-WCDMA 5MHz Signal, 9.9 dB PAR @ 0.01% CCDF test on HOTLO Application Board*




**WCDMA, ACPR_5MHz, ACPR_10MHz vs Pout**

*Test conditions unless otherwise noted: 25 °C, VDD = +48Vdc, IDQ= 450mA, Vgsp = Vgsc - 1.7V, 1C-WCDMA 5MHz Signal, 9.9 dB PAR @ 0.01% CCDF test on HOTLO Application Board*

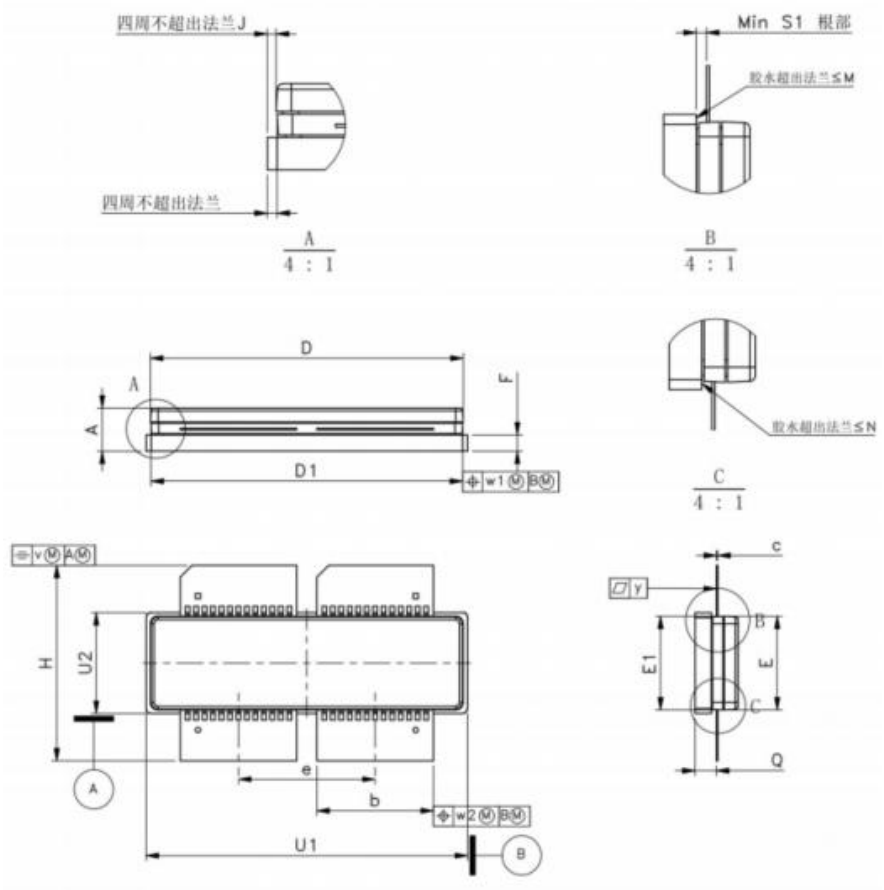
## Package Marking and Dimensions




- Line1 (fixed): Device name in W/O
- Line2 (unfixed): Marking Lot No in W/O (Sample: E596-20140001)
- Line3 (unfixed): Date Code + JY

This Marking SPEC only stipulates the content of Marking. For marking requirements such as font and size, please refer to the latest version of “Holto Product Printing Specification”

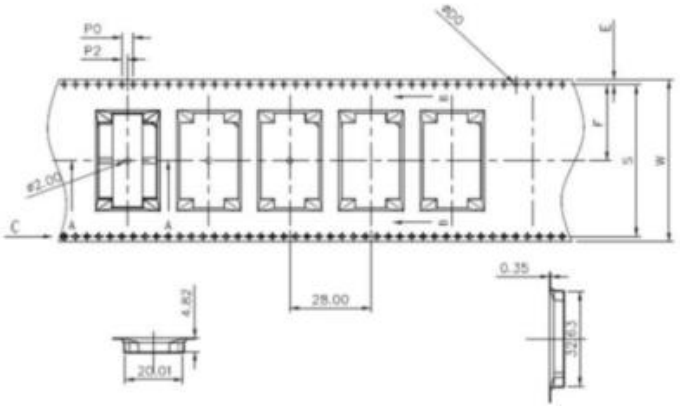
**Marking**




| Unit | | A | b | c | D | D1 | E | E1 | e | F | H | Q |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | max | 4.52 | 11.78 | 0.17 | 31.54 | 31.34 | 9.60 | 9.50 | | 1.73 | 19.71 | 2.24 |
| | nom | | | | | | | | 13.71 | | | |
| | min | 4.12 | 11.58 | 0.13 | 31.14 | 31.14 | 9.20 | 9.30 | | 1.53 | 19.51 | 2.04 |
| Unit | | U1 | U2 | J | S1 | M | N | v | w1 | w2 | y | |
| mm | max | 32.33 | 10.23 | | | | | | | | | |
| | nom | | | 0.1 | 0.5 | 0.02 | 0.1 | 0.5 | 0.5 | 0.5 | 0.1 | |
| | min | 32.13 | 10.03 | | | | | | | | | |

**Package Dimensions**

## Tape and Reel Information




| 尺寸栏 | |
|---|---|
| E | 1.75±0.10 |
| F | 26.20±0.15 |
| S | 52.40±0.10 |
| P2 | 2.00±0.10 |
| ΦDo | 1.50 +0.10 0.00 |
| ΦD1 | 2.00±0.10 |
| Po | 4.00±0.10 |
| 10Po | 40.00±0.20 |
| W | 56.00±0.30 |
| P | 28.00±0.10 |
| Ao | 20.01±0.10 |
| BO | 32.63±0.10 |
| KO | 4.82±0.10 |
| t | 0.35±0.05 |

**Tape & Reel Packaging Descriptions**

## Handling Precautions

| Parameter | Grade |
|---|---|
| Moisture Sensitivity Level MSL | 3 |

| Parameter | Rating | Standard |
|---|---|---|
| ESD – Human Body Model (HBM) | Class 1B | JESD22-A114 |
| ESD – Human Body Model (MM) | Class A | EIA/JESD22-A115 |
| ESD – Charged Device Model (CDM) | Class III | JESD22-C101 |


## RoHS Compliance

This product is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU.

## Datasheet Status

| Document status | Product status | Definition |
|---|---|---|
| Objective Datasheet | Design simulation | Product objective specification |
| Preliminary Datasheet | Customer sample | Engineering samples and first test results |
| Product Datasheet | Mass production | Final product specification |

## Abbreviations

| Acronym | Definition |
|---|---|
| LDMOS | Laterally-Diffused Metal-Oxide Semiconductor |
| CW | Continuous Waveform |

## Revision history

| Document ID | Datasheet Status | Release Date | Revision Version |
|---|---|---|---|
| Rev 1.0 | Preliminary | Dec. 2021 | Pre-release version |
| Rev 1.1 | Preliminary | Dec. 2021 | Update fin order codes |
| Rev 1.2 | Preliminary | Feb. 2022 | Supplementary BOM information |
| Rev 1.3 | Product | April 2022 | |
| Rev 1.4 | Product | April 2022 | Update company logo and English name |
| Rev 1.5 | Product | April 2022 | Update BOM |
| Rev 1.6 | Product | March 2023 | New format based on English version datasheet |

## Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations and information about HOTLO:

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