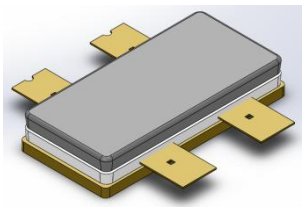
HTH9G09P550S

550W, 700 - 960 MHz LDMOS Amplifier

Product datasheet

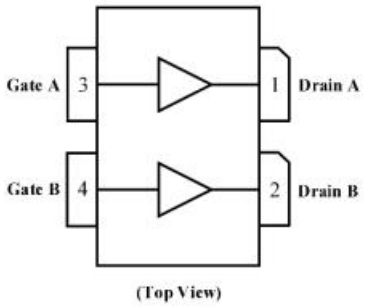
Description

The HTH9G09P550S is a unmatched discrete LDMOS Power Amplifier with 550W saturated output power covering frequency range from 700 - 960 MHz.



ACS2110S-4L RoHS compliant

Earless Flanged
Air Cavity Spliced Package; 4 Leads



Note: Exposed backside of the package is the source terminal for the transistor

Pin Connections

Features

- Operating Frequency Range: 700 - 960 MHz
- Operating Drain Voltage: +48V
- Saturation Output Power: 550W
- Power Average: 79.4W
- Device can be used on a single-ended or in a push-pull configuration. Doherty application applicable
- Excellent thermal stability due to low thermal resistance package
- Enhanced robustness design without device degradation
- Efficiency: 53%@960MHz, WCDMA
- Gain: 19dB@960MHz, WCDMA

Applications

- 3GPP 5G NR FR1 n5/8/12/13/14/18/20/26/28/29/67/85/100
- 4G-LTE B5/8/12/13/14/17/18/19/20/26/28/67/85/103
- Amplifier for Micro and Macro Base Stations
- Repeaters/DAS
- Mobile Infrastructure

Ordering Information

Part Number	Description
HTH9G09P550S	Reel Package
HTH9G09P550SEVB	925 - 960 MHz EVB

Typical Performance

RF Characteristics (Pulsed CW)

Freq (MHz)	P5dB (dBm)	Gain (dB)	Eff (%) @P5dB	Eff (%) @49dBm	IRL (dB)
925	58.1	18.84	60.88	54.0	11
942	57.7	19.36	63.82	53.4	13
960	57.4	19.57	62.81	53.9	15

Test conditions unless otherwise noted: 25 °C, VDD = +48Vdc, IDQ_Carrier= 400mA, Vgsp = Vgsc - 1.8V, PW = 100us, DC= 10% test on HOTLO Application Board

RF Characteristics (WCDMA)

Freq (MHz)	Gain (dB)	Eff (%)	ACPR* @5MHz (dBc)	ACPR* @10MHz (dBc)	IRL (dB)
925	18.56	52.5	-23.94	-39.83	11
942	18.94	52.9	-24.13	-39.81	13
960	19.01	53.7	-24.16	-39.01	15

Test conditions unless otherwise noted: 25 °C, VVDD = +48Vdc, IDQ_Carrier= 400mA, Vgsp = Vgsc - 1.8V, P_{AVG} = 49 dBm 1C-WCDMA 5MHz Signal, 9.9 dB PAR @ 0.01% CCDF test on HOTLO Application Board

**Uncorrected DPD*

Absolute Maximum Ratings

Parameter	Range/Value	Unit
Drain voltage (V_{DSS})	-0.5 to +120	V
Gate voltage (V_{GS})	-5 to +10	V
Storage Temperature (T_{STG})	-55 to +150	°C
Junction Temperature (T_J)	-40 to +225	°C

Electrical Specification

DC Characteristics (Carrier)

Parameter	Conditions	Min	Typ	Max	Unit
Breakdown Voltage $V_{(BR)DSS}$	Vgs=0V, Ids=156uA	120	-	-	V
Gate-Source Threshold Voltage $V_{GS(th)}$	Vgs=10V, Ids=156uA	2.2	2.7	3.0	V
Drain Leakage Current I_{DSS}	Vgs=0V, Vds=110V	-	-	500	nA
Gate Leakage Current I_{GSS}	Vgs=10V, Vds=0V	-	-	500	nA

DC Characteristics (Peak)

Parameter	Conditions	Min	Typ	Max	Unit
Breakdown Voltage $V_{(BR)DSS}$	Vgs=0V, Ids=260uA	120	-	-	V
Gate-Source Threshold Voltage $V_{GS(th)}$	Vgs=10V, Ids=260uA	2.2	2.7	3.0	V
Drain Leakage Current I_{DSS}	Vgs=0V, Vds=110V	-	-	500	nA
Gate Leakage Current I_{GSS}	Vgs=10V, Vds=0V	-	-	500	nA

RF Characteristics (Pulsed CW)

Parameter	Conditions	Min	Typ	Max	Units
Frequency Range	Pout=49 dBm	0.925	/	0.96	GHz
P5dB	Freq=0.96GHz	56.8	57.3	/	dBm

Test conditions, unless otherwise noted: 25 °C, VDD=+48Vdc, IDQ = 400 mA, Vgsp=Vgsm-1.8V, Pulse Width = 100 us, Duty Cycle = 10%,Based on FT board

RF Characteristics (WCDMA)

Parameter	Conditions	Min	Typ	Max	Units
Frequency Range	Pout=49 dBm	0.925	/	0.96	GHz
Gain	Freq=0.96 GHz, Pout=49 dBm	17	19	22	dB
Eff	Freq=0.96 GHz, Pout=49 dBm	48	52	60	%
ACLR@5MHz	Freq=0.96 GHz, Pout=49 dBm	-40	-27	-23	dBc

Test conditions, unless otherwise noted: 25 °C, VDD=+48Vdc, IDQ = 400 mA, Vgsp=Vgsm-1.8V, single-carrier, 5MHz WCDMA signal with 9.9 dB PAR @ 0.01% CCDF Based on FT board

RF Characteristics (Small-Signal)

Parameter	Conditions	Min	Typ	Max	Units
Input Return Loss	Freq=0.96 GHz	/	-9	-8	dB

Test conditions, unless otherwise noted: 25 °C, VDD=+48Vdc, IDQ = 400 mA, Vgsp=Vgsm-1.8V, CW, Based on FT board

Load Mismatch Test

Condition	Test Result
VSWR=10:1, at all Phase Angles, VDD = +48Vdc, IDQ_Carrier= 400mA, Vgsp = Vgsc - 1.8V, 1C-WCDMA 5MHz Signal, 9.9 dB PAR, P_{AVG} = 52 dBm, Frequency 942 MHz test on HOTLO Application Board	No Device Degradation

Thermal Information

Parameter	Condition	Value (Typ)	Unit
Thermal Resistance Junction to Case (R_{TH})	T_{CASE}= 80°C, VDD = +48Vdc, IDQ_Carrier= 400mA, 1C-WCDMA 5MHz Signal, 9.9 dB PAR, P_{AVG} = 49 dBm	0.46	°C /W

Load Pull Performance Carrier

Test conditions unless otherwise noted: 25 °C, VDD = +48Vdc, IDQ= 400mA, PW = 40us, DC= 4%

Max Output Power (Carrier)						
Freq (MHz)	Z_source (Ω)	Z_load [1] (Ω)	Gain (dB)	P3dB (dBm)	P3dB (W)	Eff (%)
760	2.18-j*0.8	2.17-j*0	24.7	55.0	321	68.5
860	2.45-j*4.1	1.9-j*0.3	23.2	54.9	312	64.1
960	5-j*8.9	1.7-j*0.43	22.6	54.8	305	64.3

[1] Load impedance for optimum P3dB pout

Max Drain Efficiency (Carrier)						
Freq (MHz)	Z_source (Ω)	Z_load [2] (Ω)	Gain (dB)	P3dB (dBm)	P3dB (W)	Eff (%)
760	2.18-j*0.8	2.13+j*1.5	26.6	53.7	234	77.3
860	2.45-j*4.1	1.5+j*1.1	25.5	53.3	215	74.8
960	5-j*8.9	1.7+j*0.5	24.5	53.8	240	72.2

[2] Load impedance for optimum P3dB efficiency

Load Pull Performance Peak

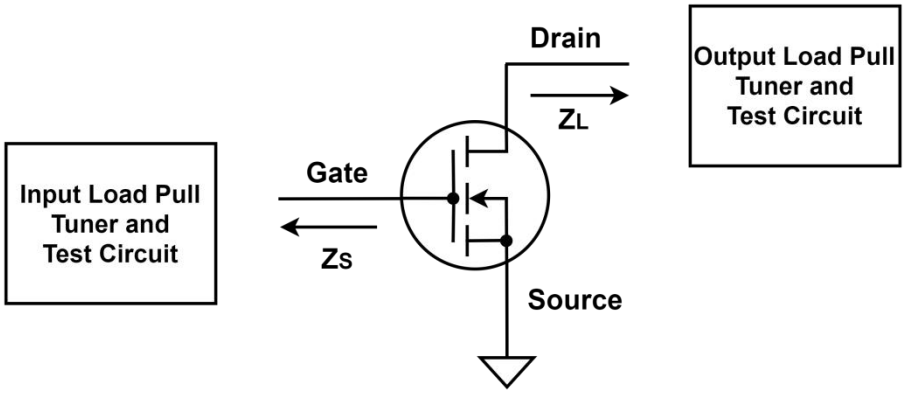
Test conditions unless otherwise noted: 25 °C, VDD = +48Vdc, IDQ= 500mA, PW = 40us, DC= 4%

Max Output Power (Peak)						
Freq (MHz)	Z_source (Ω)	Z_load [1] (Ω)	Gain (dB)	P3dB (dBm)	P3dB (W)	Eff (%)
760	1.8-j*2.7	1.4-j*0.54	24.3	56.8	482	67.5
860	2.14-j*5.7	1.4-j*1	22.6	56.7	468	62.2
960	5.3-j*13.13	1.5-j*0.89	21.5	56.9	485	63.6

[1] Load impedance for optimum P3dB pout

Max Drain Efficiency (Peak)						
Freq (MHz)	Z_source (Ω)	Z_load [2] (Ω)	Gain (dB)	P3dB (dBm)	P3dB (W)	Eff (%)
760	1.8-j*2.7	1.2+j*0.5	26.0	55.0	321	75.2
860	2.14-j*5.7	1.16+*j0	24.5	55.6	363	72.5
960	5.3-j*13.13	1.17-j*0.24	23.7	55.4	347	68.8

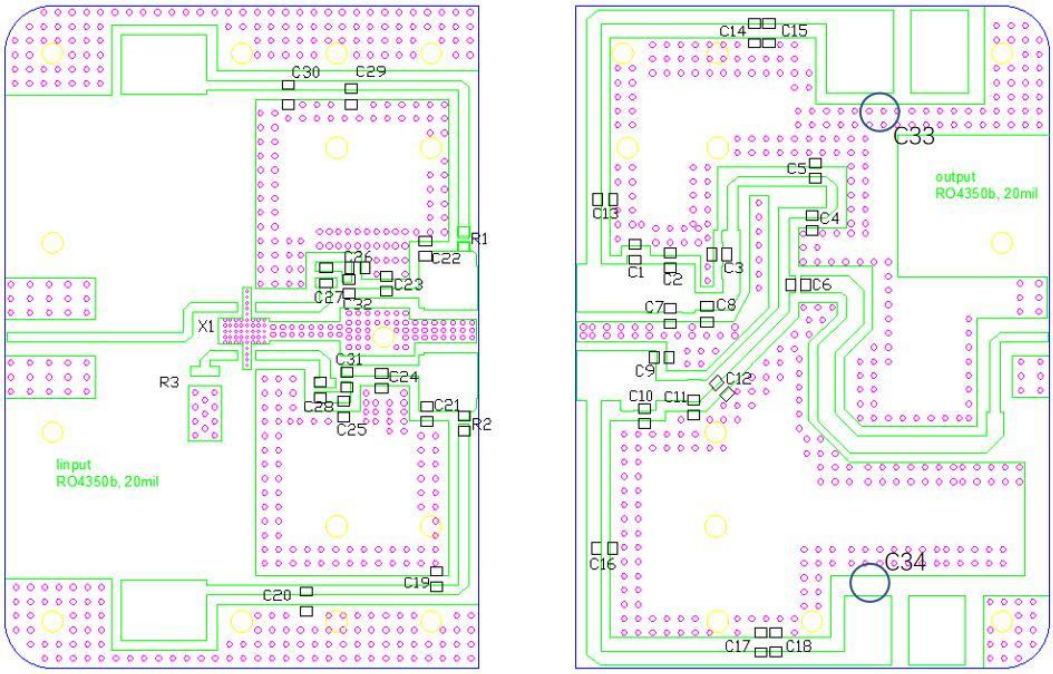
[2] Load impedance for optimum P3dB efficiency



Z_source : Measured impedance presented to the input of the device at the package reference plane

Z_load : Measured impedance presented to the output of the device at the package reference plane

HTH9G09P550S 925- 960 MHz Reference Design



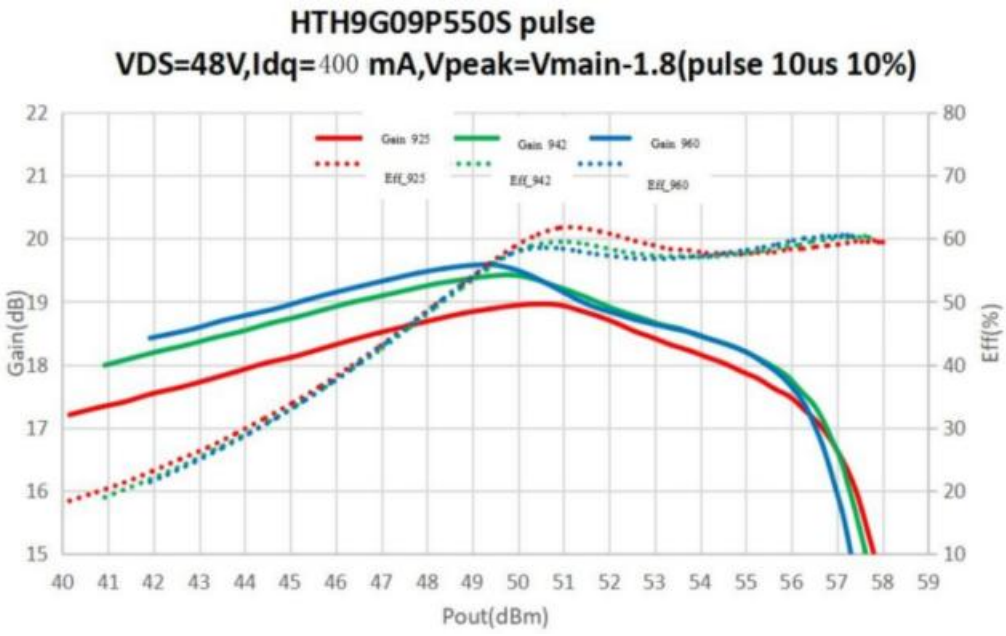
EVB Layout

Bill of Materials (BoM) - HTH9G09P550S 925- 960 MHz Reference Design

Reference	Value	Description	Manufacturer	P/N
Q1	-	550W, 700 - 960 MHz LDMOS PA	Holto	HTH9G09P550S
C6,C13,C16,C19, C27,C28,C29,C31 ,C32	56pF	MLCC	Murata	GQM2195C2E560JB12
C1,C7	9p1F	MLCC	Murata	GQM2195G2E9R1BB12
C2	6p8F	MLCC	Murata	GQM2195G2E6R8BB12
C3	5p6F	MLCC	Murata	GQM2195G2E5R6BB12
C4,C5	2pF	MLCC	Murata	GQM2195G2E2R0BB12
C8,C11	7p5F	MLCC	Murata	GQM2195G2E7R5BB12
C10	10pF	MLCC	Murata	GQM2195C2E100JB12
C12,C23,C24	3p3F	MLCC	Murata	GQM2195G2E3R3BB12

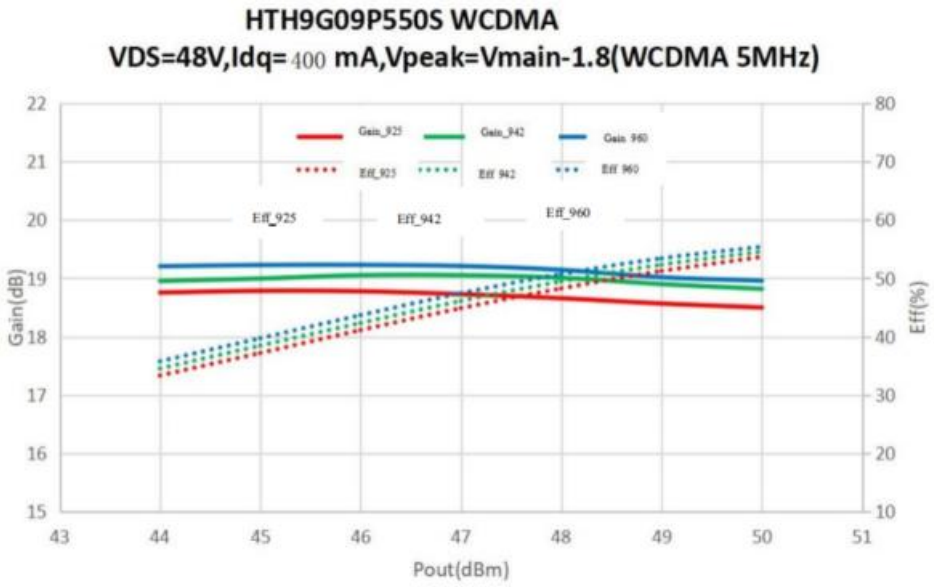
Reference	Value	Description	Manufacturer	P/N
C21	2p7F	MLCC	Murata	GQM2195G2E2R7BB12
C22,C25,C26	2p2F	MLCC	Murata	GQM2195G2E2R2BB12
C14,C17	4u7F /100V	MLCC	Murata	GRM32DC72A475ME01
C15,C18,C20, C30	10uF /100V	MLCC	Murata	GRM32EC72A106KE05
C33,C34	220uF /100V	Electrolytic Capacitor	Vishay	MAL213669221E3
R1, R2	10Ω	Thick Film Resistor	YAGEO	RC0805FR-0710RL
R3	50Ω/ 25W	High Frequency/RF Resistors	ANAREN	C16A50Z4
X1	-	Hybrid Coupler 5dB, 90°	ANAREN	X3C07F1-05S
PCB	Rogers 4350B (er = 3.66), 20 mil (0.508 mm), 35 µm (1oz)			

Performance Plots



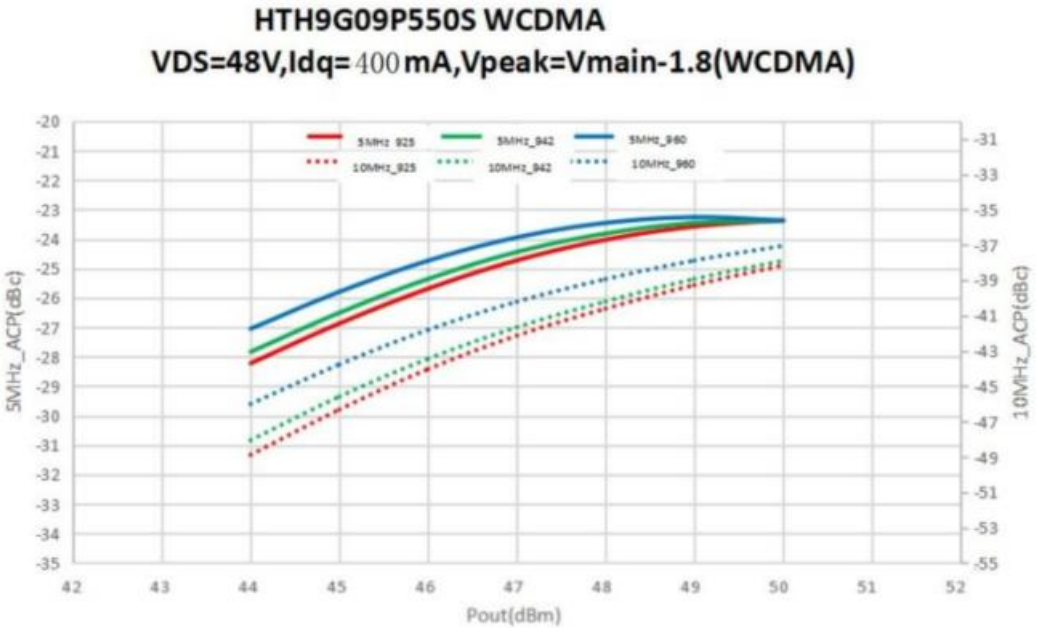
Pulsed CW, Gain and Efficiency vs Pout

Test conditions unless otherwise noted: 25 °C, VDD = +48Vdc, IDQ= 400mA, Vgsp = Vgsc - 1.8V, PW = 100us, DC= 10% test on HOTLO Application Board



WCDMA, Gain and Efficiency vs Pout

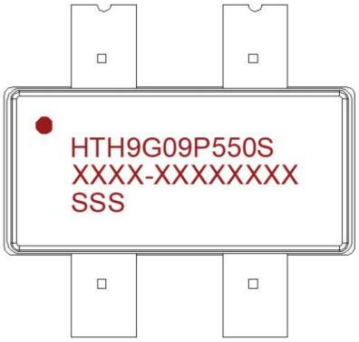
Test conditions unless otherwise noted: 25 °C, VDD = +48Vdc, IDQ = 400mA, Vgsp = Vgsc - 1.8V, 1C-WCDMA 5MHz Signal, 9.9 dB PAR @ 0.01% CCDF test on HOTLO Application Board



WCDMA, ACPR_5MHz, ACPR_10MHz vs Pout

Test conditions unless otherwise noted: 25 °C, VDD = +48Vdc, IDQ= 400mA, Vgsp = Vgsc - 1.8V, 1C-WCDMA 5MHz Signal, 9.9 dB PAR @ 0.01% CCDF test on HOTLO Application Board

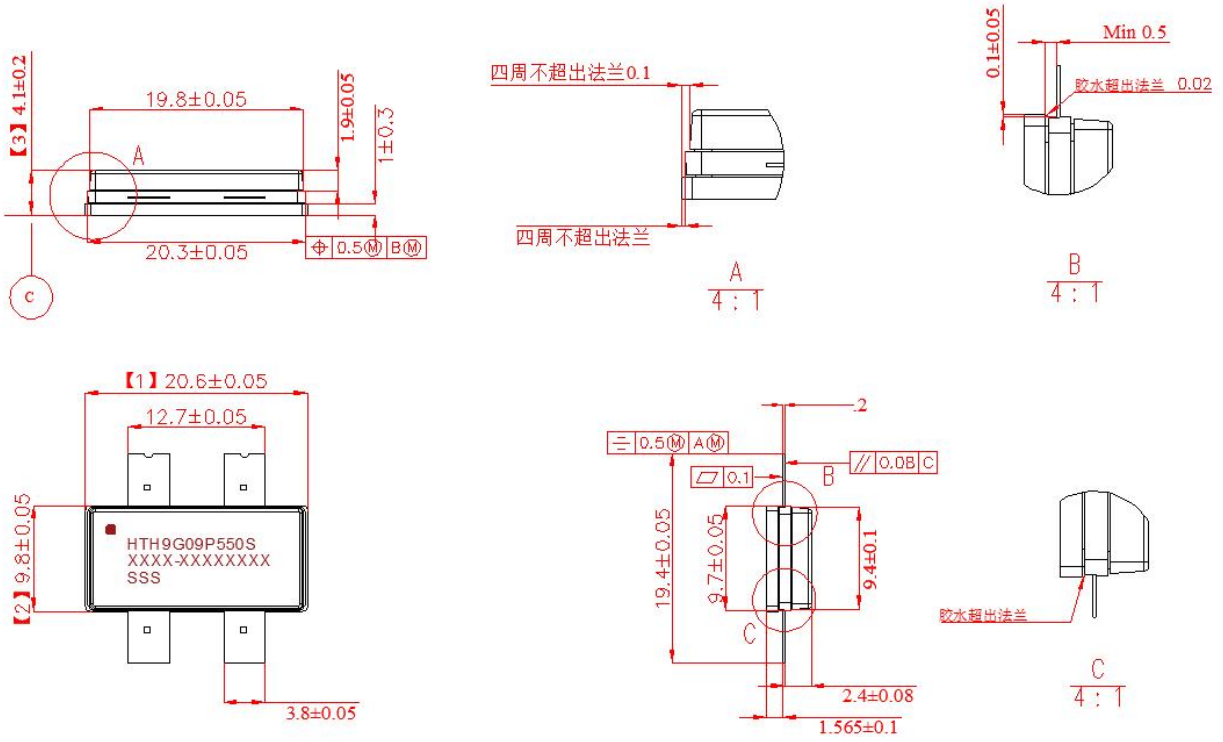
Package Marking and Dimensions



- Line1 (fixed): Device name in W/O
- Line2 (unfixed): Marking Lot No in W/O (Sample: E596-20140001)
- Line3 (unfixed): Date Code + JY

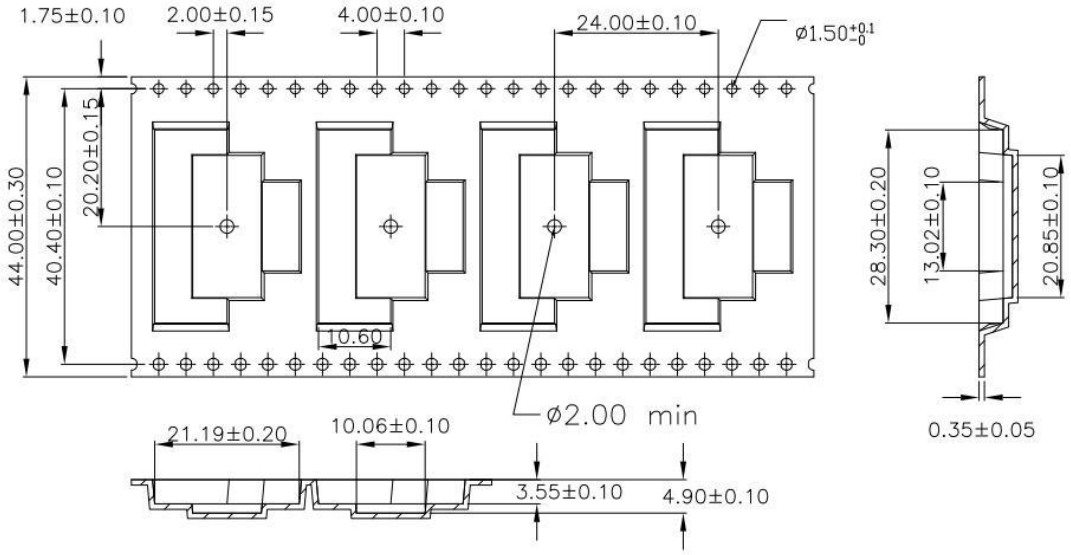
This Marking SPEC only stipulates the content of Marking. For marking requirements such as font and size, please refer to the latest version of "Holto Product Printing Specification"

Marking



Package Dimensions

Tape and Reel Information



Handling Precautions

Parameter	Grade
Moisture Sensitivity Level MSL	2

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 1B	JESD22-A114
ESD – Human Body Model (MM)	Class A	EIA/JESD22-A115
ESD – Charged Device Model (CDM)	Class III	JESD22-C101

RoHS Compliance

This product is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU.

Datasheet Status

Document status	Product status	Definition
Objective Datasheet	Design simulation	Product objective specification
Preliminary Datasheet	Customer sample	Engineering samples and first test results
Product Datasheet	Mass production	Final product specification

Abbreviations

Acronym	Definition
LDMOS	Laterally-Diffused Metal-Oxide Semiconductor
CW	Continuous Waveform

Revision history

Document ID	Datasheet Status	Release Date	Revision Version
Rev 1.0	Preliminary	Dec. 2021	Preliminary
Rev 1.1	Preliminary	Feb. 2022	Update fin order codes
Rev 1.2	Preliminary	April 2022	Update company logo and English name
Rev 1.3	Preliminary	May 2022	Updated Thermal Resistance, Package and Mark information
Rev 1.4	Product	June 2022	Updated RF reference circuits, test data, electrical characteristics and moisture sensitivity information
Rev 1.5	Product	Nov. 2022	Update limit parameters, electrical characteristics
Rev 1.6	Product	March 2023	New format based on English version datasheet
Rev 1.7	Product	April 2024	Updata mark

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations and information about HOTLO:

- Web: www.andesource.com
- Email: andehk@andesource.com

For technical questions and application information:

- Email: andetech@andesource.com

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