

Description

The HTA50P3 is a GaAs Wide Bandwidth, High Gain, High Linearity Driver IC in a 16-pin 3x3 mm QFN package. The chip covers 1800 - 5000 MHz frequency range with 29 dB Gain and 35 dBm OIP3.

Features

- Operating Frequency Range: 1800 - 5000 MHz
- Operating Drain Voltage: +5V
- High/Low Power Modes
- 50 Ω Input/Output
- Psat_High Mode: 25 dBm
- High Mode Gain: 29 dB
- Psat_Low Mode: 22.5 dBm
- Low Mode Gain: 28 dB

Applications

- Small cell and Micro cell pre-Driver
- DAS (Distributed Antenna System)
- AAS (Active Antenna System)

Ordering Information

Part Number	Description
HTA50P3	Reel Package
HTA50P3EVB	HTA50P3 EVB



Typical Performance 1800 - 4000 MHz

Parameter	Conditions	Min	Typ.	Max	Unit
High Power Mode					
Frequency	50 Ω Input/Ouput	1800		4000	MHz
Gain	$P_{IN} = -20$ dBm	27	29	-	dB
Gain Flatness	600 MHz BW	-	1	1.5	dB
IRL		8	10	-	dB
ORL		8	10	-	dB
ISO		32	35	-	dB
P1dB		22.5	24	-	dBm
Psat		23.5	25	-	dBm
OIP3	$P_{out} = +2$ dBm/tone, $\Delta F = 1$ MHz	32	35	-	dBm
Current Consumption		120	140	150	mA
NF		-	5	6	dB

Test conditions unless otherwise noted: 25 °C, VDD = STBY = +5Vdc test on HOTLO Application Board

Parameter	Conditions	Min	Typ.	Max	Unit
Low Power Mode					
Frequency	50 Ω Input/Ouput	1800		4000	MHz
Gain	$P_{IN} = -20$ dBm	26	28		dB
Gain Flatness	600 MHz BW	-	1	1.5	dB
IRL		8	10	-	dB
ORL		8	10	-	dB
ISO		32	35	-	dB
P1dB		20.5	21.5	-	dBm
Psat		21.5	22.5	-	dBm
OIP3	$P_{out} = +2$ dBm/tone, $\Delta F = 1$ MHz	32	33	-	dBm
Current Consumption		75	90	105	mA
NF		-	5	6	dB

Test conditions unless otherwise noted: 25 °C, VDD = STBY = +5Vdc test on HOTLO Application Board

Typical Performance 4000 - 5000 MHz

Parameter	Conditions	Min	Typ.	Max	Unit
High Power Mode					
Frequency	50 Ω Input/Ouput	4000		5000	MHz
Gain	$P_{IN} = -20$ dBm	26	28.0	-	dB
Gain Flatness	600 MHz BW	-	1	1.5	dB
IRL		8	10	-	dB
ORL		8	10	-	dB
ISO		34	40	-	dB
P1dB		22	23	-	dBm
Psat		22.5	24	-	dBm
OIP3	$P_{out} = +2$ dBm/tone, $\Delta F = 1$ MHz	32	35	-	dBm
Current Consumption		125	145	155	mA
NF		-	5	6	dB

Test conditions unless otherwise noted: 25 °C, VDD = STBY = +5Vdc test on HOTLO Application Board

Parameter	Conditions	Min	Typ.	Max	Unit
Low Power Mode					
Frequency	50 Ω Input/Ouput	4000		5000	MHz
Gain	$P_{IN} = -20$ dBm	25	27.0	-	dB
Gain Flatness	600 MHz BW	-	1	1.5	dB
IRL		8	10	-	dB
ORL		8	10	-	dB
ISO		34	35	-	dB
P1dB		20	21	-	dBm
Psat		20.5	22	-	dBm
OIP3	$P_{out} = +2$ dBm/tone, $\Delta F = 1$ MHz	30	33	-	dBm
Current Consumption		75	90	105	mA
NF		-	5	6	dB

Test conditions unless otherwise noted: 25 °C, VDD = STBY = +5Vdc test on HOTLO Application Board

Absolute Maximum Ratings

Parameter	Range/Value	Unit
Max Pin	20	dBm
Operation voltage (V_{CC})	≤ 5.5	V
Storage Temperature (T_{STG})	-55 to +150	$^{\circ}C$
Junction Temperature (T_J)	-40 to +150	$^{\circ}C$

Electrical Specification

DC Characteristics

Parameter	Conditions	Min	Typ	Max	Unit
Drain Leakage Current I_{DSS}	STBY = 0V RF _{OUT} = 5V V_{BIAS} = 5V	-	230	-	μA
Gate Leakage Current I_{GSS}	STBY = 0V RF _{OUT} = 5V V_{BIAS} = 5V	-	2	-	mA
Rise Time T_{RISE}	50% STBY-10/90% RF	-	500	-	ns
Fall Time T_{FALL}	50% STBY-90/10% RF	-	500	-	ns

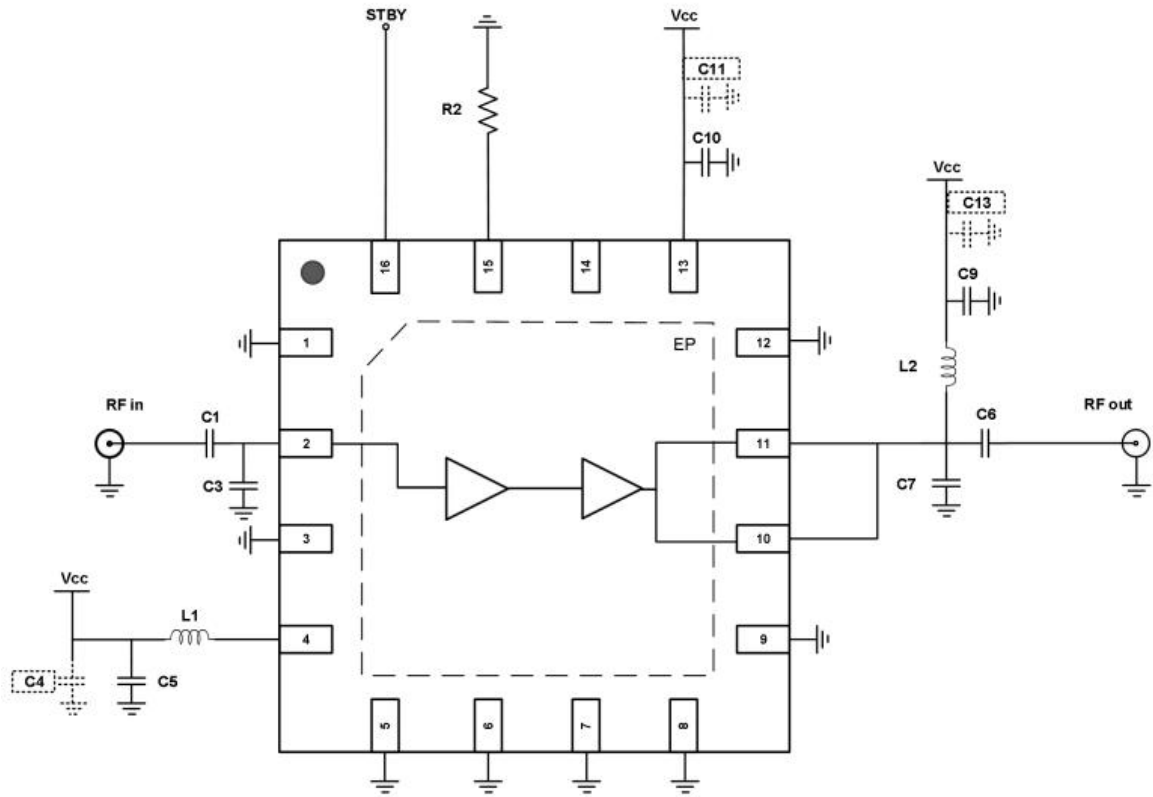
Load Mismatch Test

Condition	Test Result
VSWR=20:1, at all Phase Angles, VDD = +5Vdc, IDQ= 130mA, CW signal Pout = 24 dBm (1dB input Overdrive from P1dB) @1800 MHz test on HOTLO Application Board	No Device Degradation
VSWR=20:1, at all Phase Angles, VDD = +5Vdc, IDQ= 130mA, CW signal Pout = 24 dBm (1dB input Overdrive from P1dB) @2600 MHz test on HOTLO Application Board	No Device Degradation

Thermal Information

Parameter	Condition	Value (Typ)	Unit
Thermal Resistance Junction to Case (R_{TH})	T_{CASE} = 25 $^{\circ}C$, CW signal 0.25W	49.8	$^{\circ}C/W$

HTA50P3 1800 - 4000 MHz Reference Design

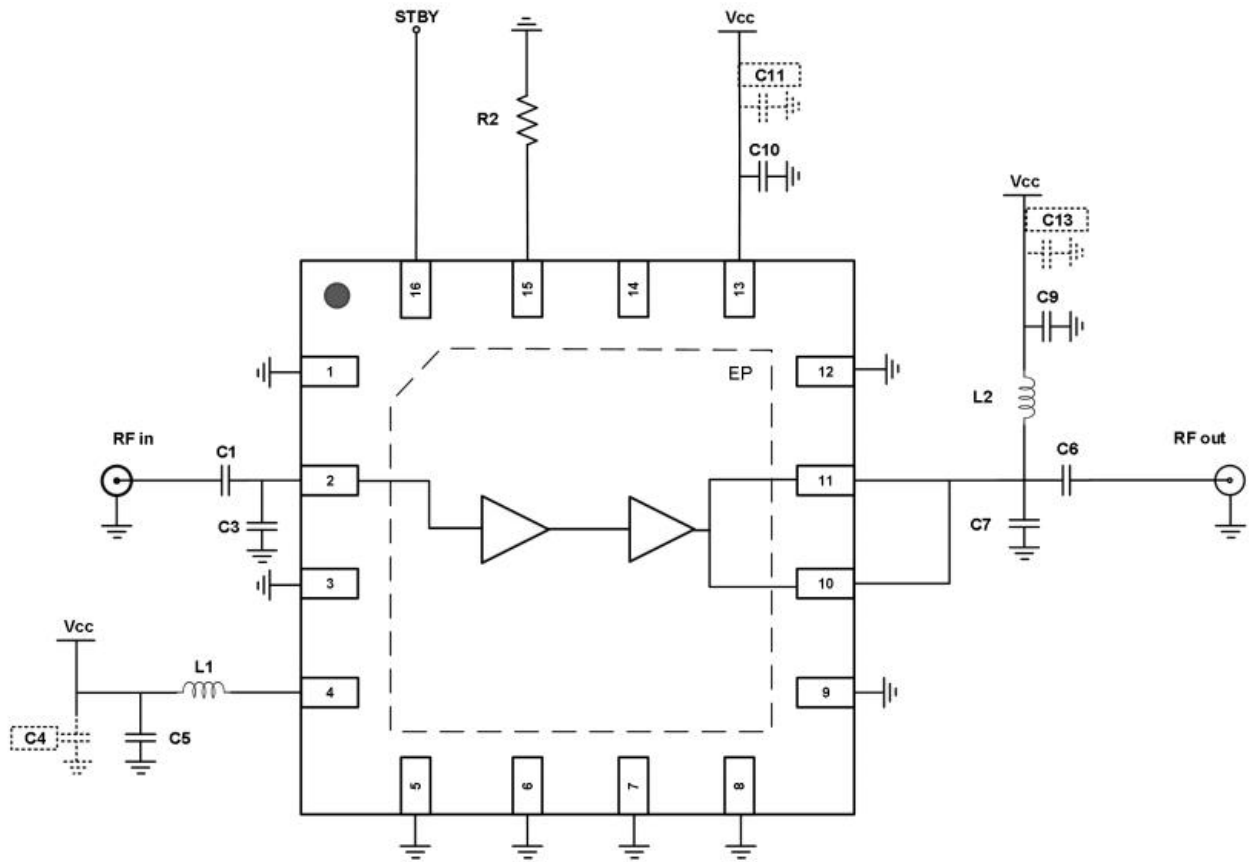


EVB Schematic 1800 - 4000 MHz

Bill of Materials (BoM) - HTA50P3 1800 - 4000 MHz Reference Design

Reference	Value	Description	Manufacturer	P/N
Q1	-	1800 - 5000 MHz GaAs MMIC Amplifier	Holto	HTA50P3
C1, C5, C6, C9, C11	100pF	MLCC	Murata	GRM1555C1H101GA01
C2, C8, C12	NM	-	-	-
C3	0p4F	MLCC	Murata	GRM1555C1HR40WA01
C4, C10, C13	1uF	MLCC	Murata	GRM155C81E105KE11
C7	0p3F	MLCC	Murata	GRM1555C1HR30WA01
L1	3n3H	Chip Inductor	Coilcraft	0402HP_3N3XJEU
L2	12nH	Chip Inductor	Coilcraft	0402CS_12NXJLU
R1	0 Ω	Thick Film Resistor	-	0402
R2	2.4 kΩ High Power Mode 20 kΩ Low Power Mode	Thick Film Resistor	-	0402
R3	NM	-	-	-
R4	0 Ω	Thick Film Resistor	-	0402

HTA50P3 4000 - 5000 MHz Reference Design



EVB Schematic 4000 - 5000 MHz

Bill of Materials (BoM) - HTA50P3 4000 - 5000 MHz Reference Design

Reference	Value	Description	Manufacturer	P/N
Q1	-	1800 - 5000 MHz GaAs MMIC Amplifier	Holto	HTA50P3
C1, C5, C6, C9, C11	100pF	MLCC	Murata	GRM1555C1H101GA01
C2, C8, C12	NM	-	-	-
C3	0p4F	MLCC	Murata	GRM1555C1HR40WA01
C4, C10, C13	1uF	MLCC	Murata	GRM155C81E105KE11
C7	0p6F	MLCC	Murata	GRM1555C1HR30WA01
L1	0 Ω	Thick Film Resistor	-	0402
L2	12nH	Chip Inductor	Coilcraft	0402CS_12NXJLU
R1	0 Ω	Thick Film Resistor	-	0402
R2	2.4 kΩ High Power Mode 20 kΩ Low Power Mode	Thick Film Resistor	-	0402
R3	NM	-	-	-
R4	0 Ω	Thick Film Resistor	-	0402

Performance Plots 1800 - 4000 MHz Reference Design

Figure 1 S21 Vs. Voltage – 25 °C

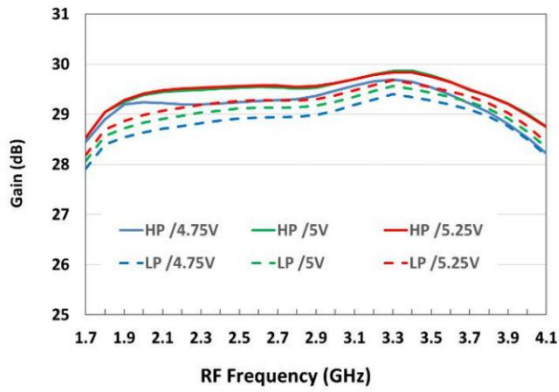


Figure 2 S11 Vs. Voltage – 25 °C

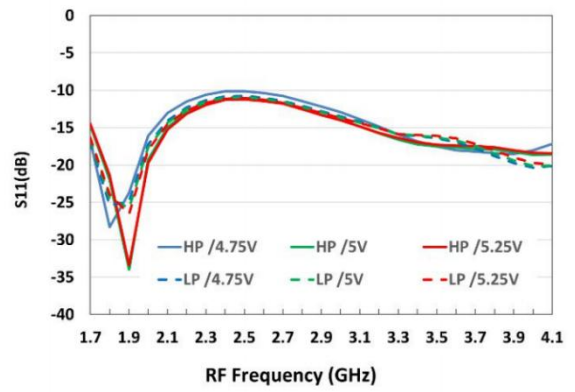


Figure 3 S12 Vs. Voltage – 25 °C

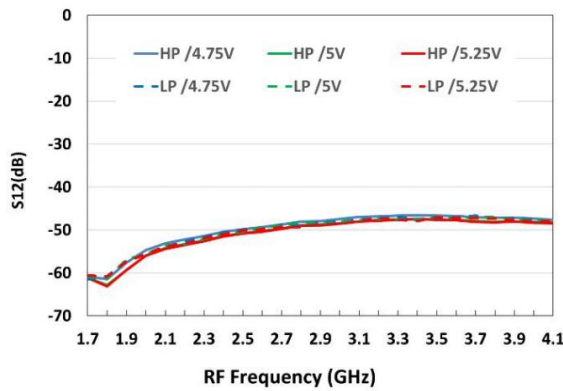


Figure 4 S22 Vs. Voltage – 25 °C

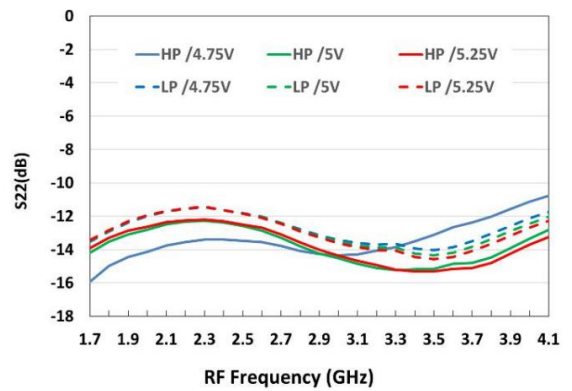


Figure 5 S21 Vs. Temp – 5V

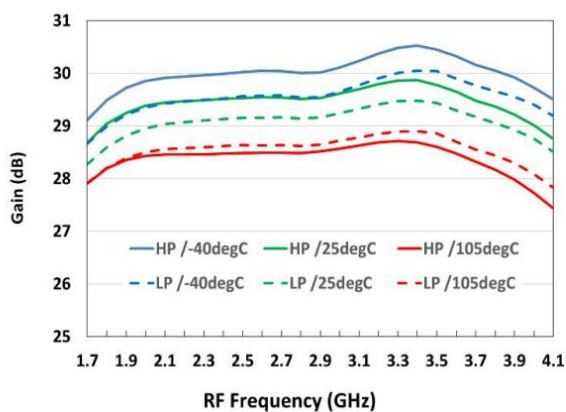


Figure 6 S11 Vs. Temp – 5V

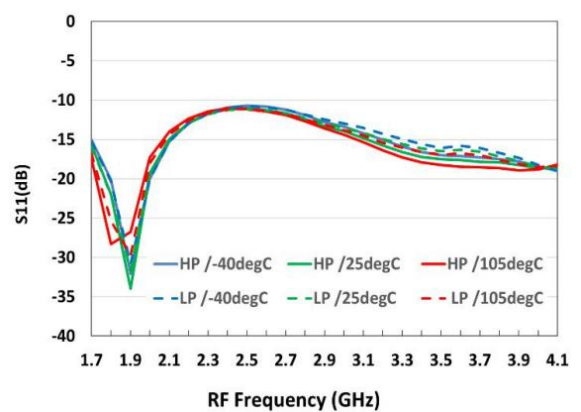


Figure 7 S12 Vs. Temp – 5V

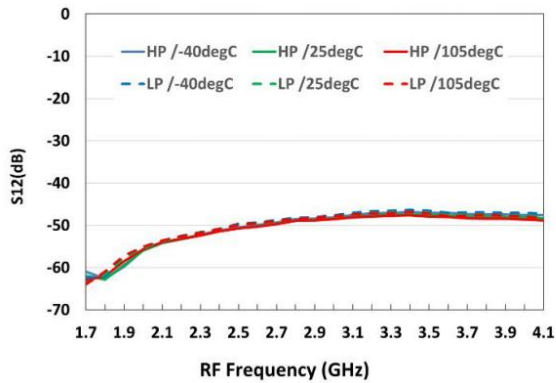
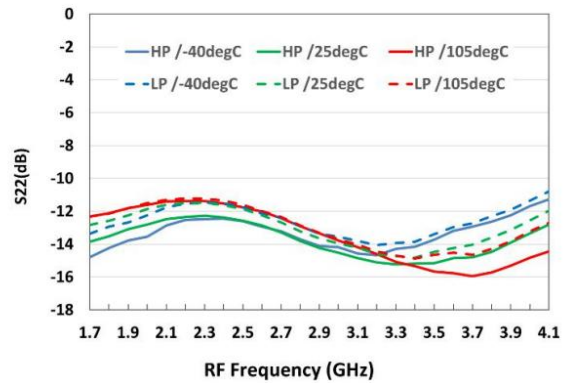


Figure 8 S22 Vs. Voltage – 5V



S Parameters

Test conditions unless otherwise noted: 25 °C, VDD = STBY = +5Vdc test on HOTLO Application Board

Figure 9. OIP3 (High Power Mode) Vs. Volt – 25 °C

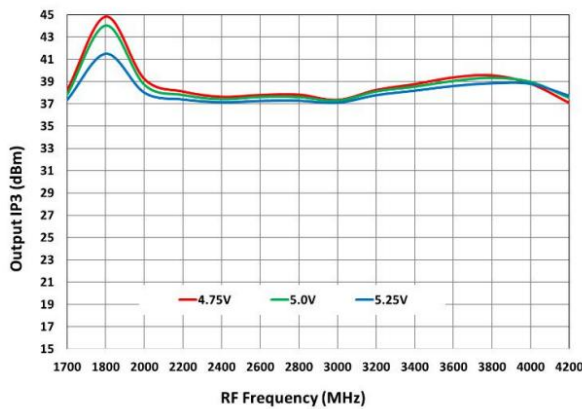


Figure 10. OIP3 (High Power Mode) Vs. Temp – 5V

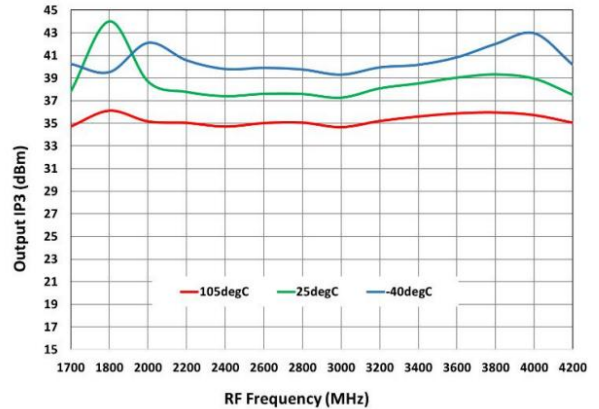


Figure 11 OIP3 (Low Power Mode) Vs. Volt – 25 °C

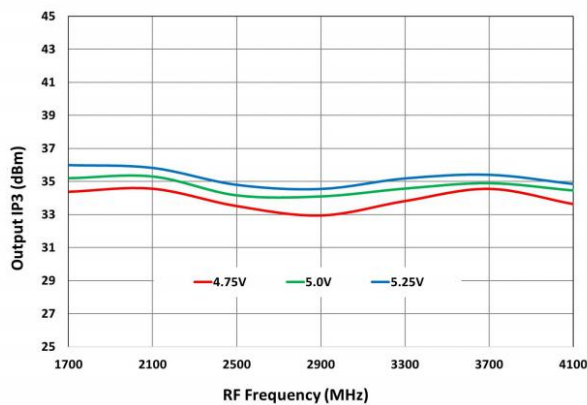
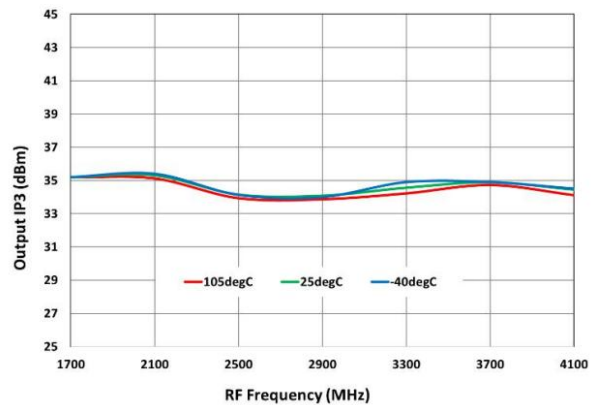


Figure 12 OIP3 (Low Power Mode) Vs. Temp – 5V



OIP3

Test conditions unless otherwise noted: 25 °C, VDD = STBY = +5Vdc test on HOTLO Application Board

Figure 13. P1dB (High Power Mode) Vs. Volt – 25 °C

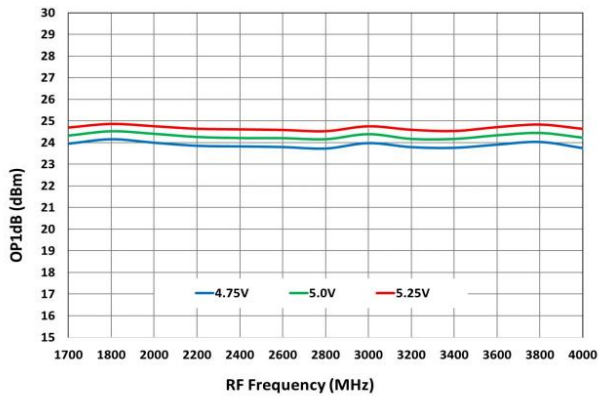


Figure 14. P1dB (High Power Mode) Vs. Temp – 5V

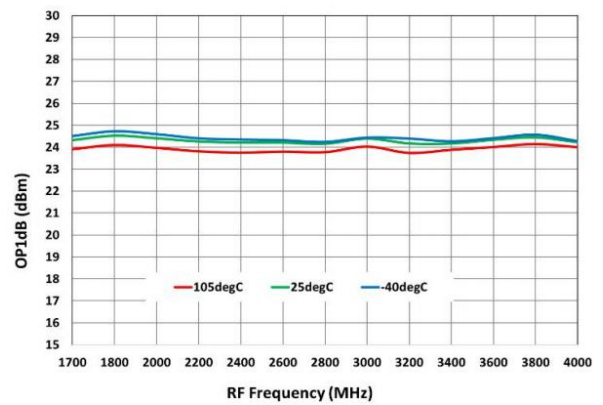


Figure 15 P1dB (Low Power Mode) Vs. Volt– 25 °C

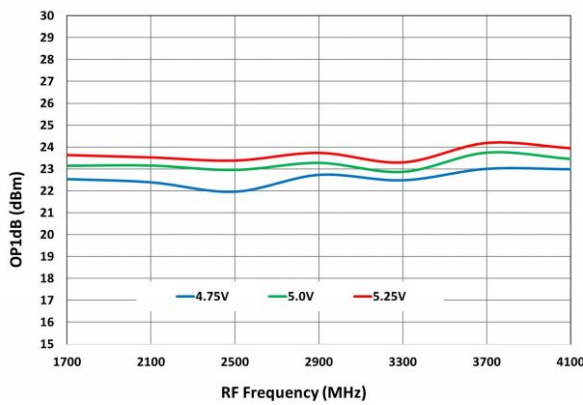
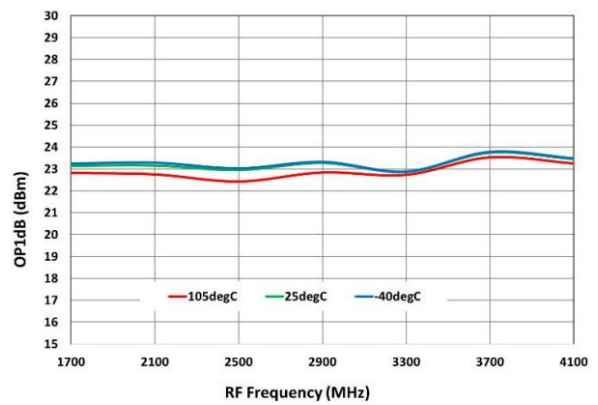


Figure 16 P1dB (Low Power Mode) Vs. Temp – 5V



P1dB

Test conditions unless otherwise noted: 25 °C, VDD = STBY = +5Vdc test on HOTLO Application Board

Figure 17 Noise Figure vs. Temp – 5V

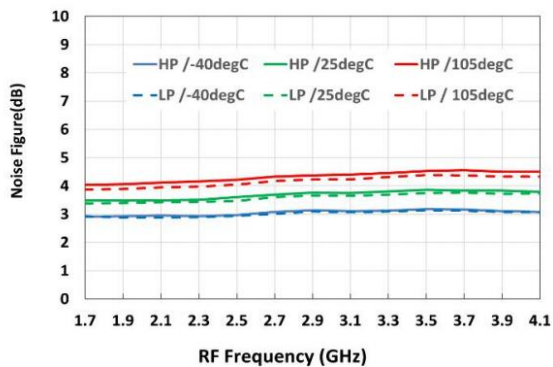
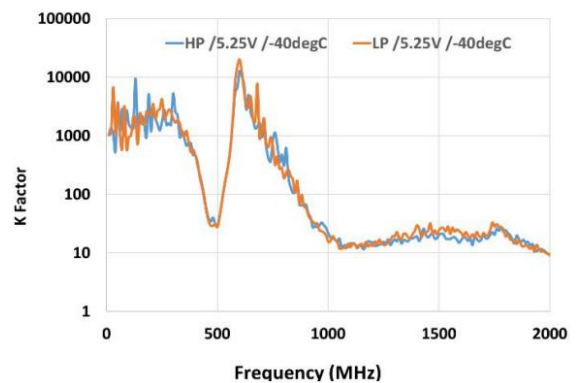


Figure 18. K Factors (Low Band)



NF & K-Factor

Test conditions unless otherwise noted: 25 °C, VDD = STBY = +5Vdc test on HOTLO Application Board

Performance Plots 4000 - 5000 MHz Reference Design

Figure 1 S21 Vs. Voltage – 25 °C

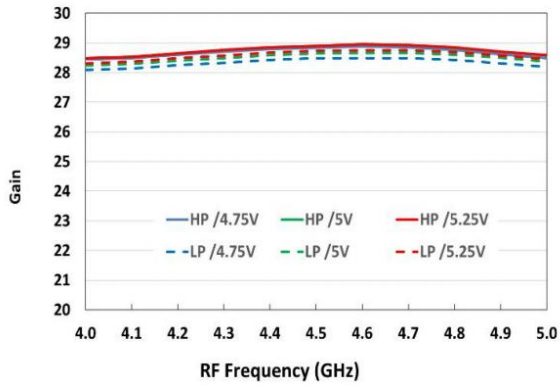


Figure 2 S11 Vs. Voltage – 25 °C

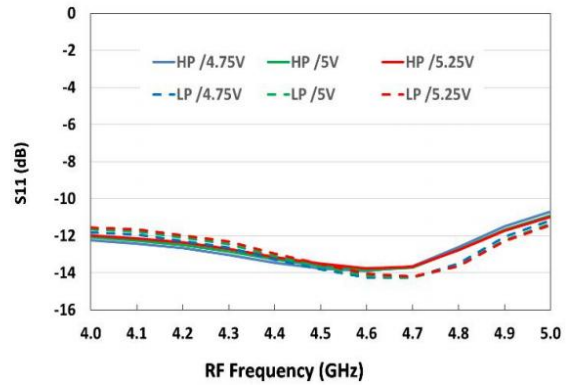


Figure 3 S12 Vs. Voltage – 25 °C

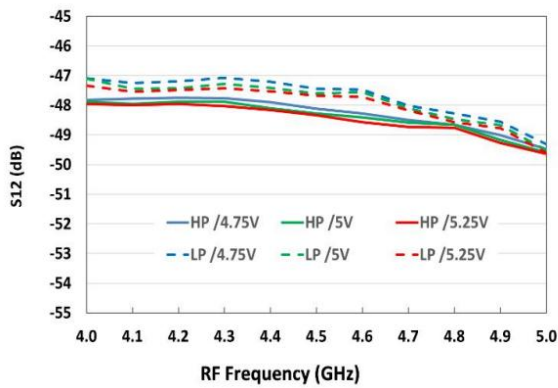


Figure 4 S22 Vs. Voltage – 25 °C

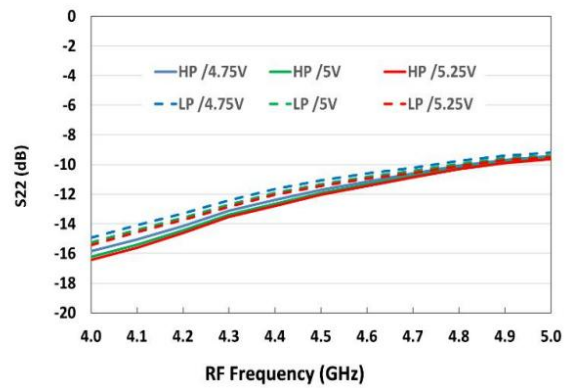


Figure 5 S21 Vs. Temp – 5V

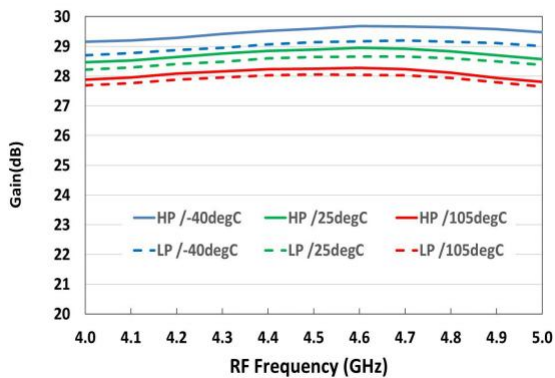


Figure 6 S11 Vs. Temp – 5V

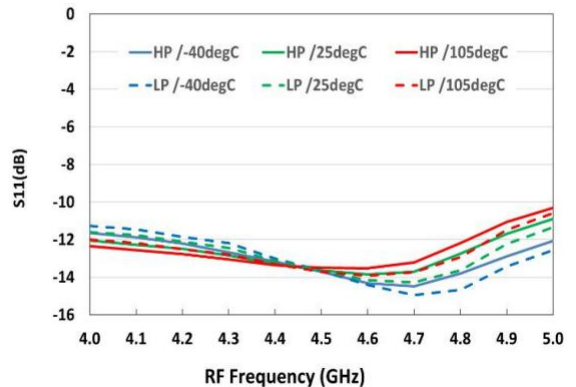


Figure 7 S12 Vs. Temp – 5V

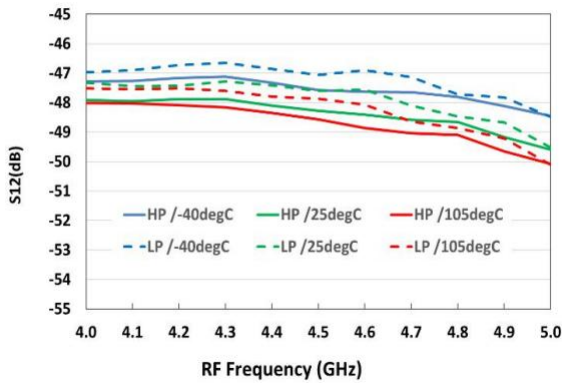
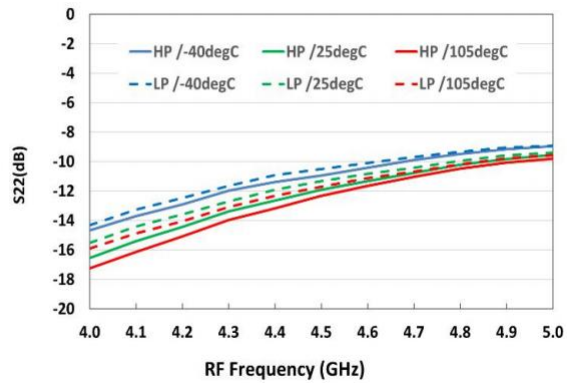


Figure 8 S22 Vs. Temp – 5V



S Parameters

Test conditions unless otherwise noted: 25 °C, VDD = STBY = +5Vdc test on HOTLO Application Board

Figure 9. OIP3 (High Power Mode) Vs. Volt – 25 °C

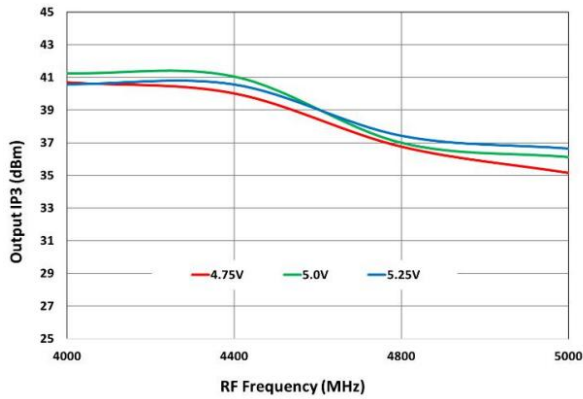


Figure 10. OIP3 (High Power Mode) Vs. Temp – 5V

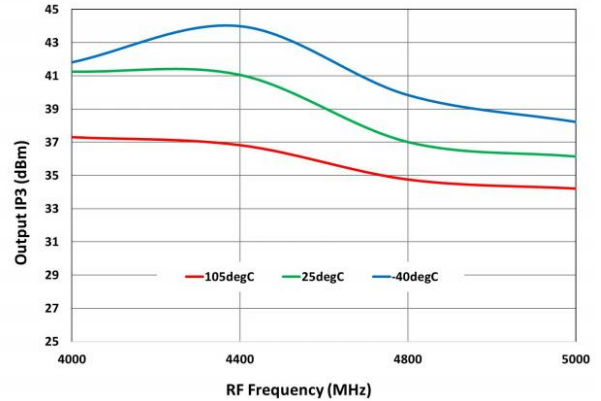


Figure 11 OIP3 (Low Power Mode) Vs. Volt – 25 °C

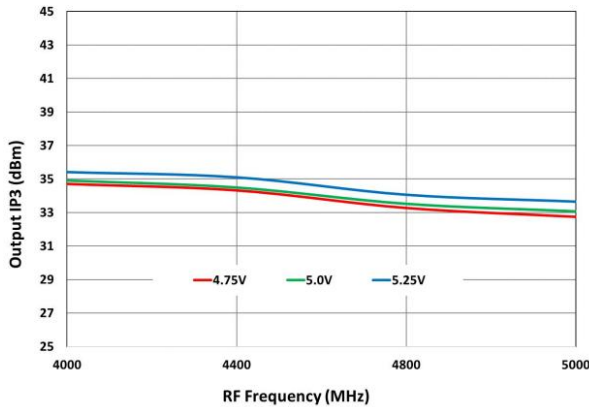
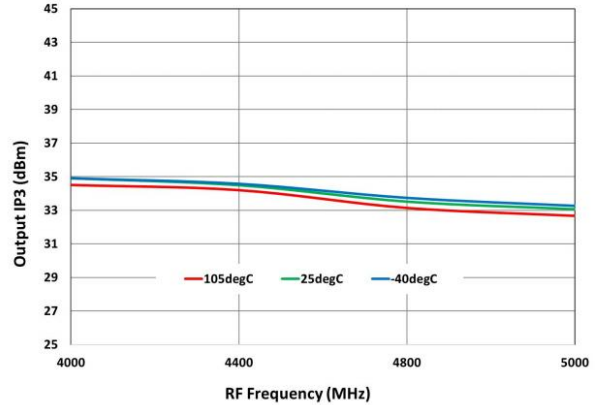


Figure 12 OIP3 (Low Power Mode) Vs. Temp – 5V



OIP3

Test conditions unless otherwise noted: 25 °C, VDD = STBY = +5Vdc test on HOTLO Application Board

Figure 13. P1dB (High Power Mode) Vs. Volt – 25 °C

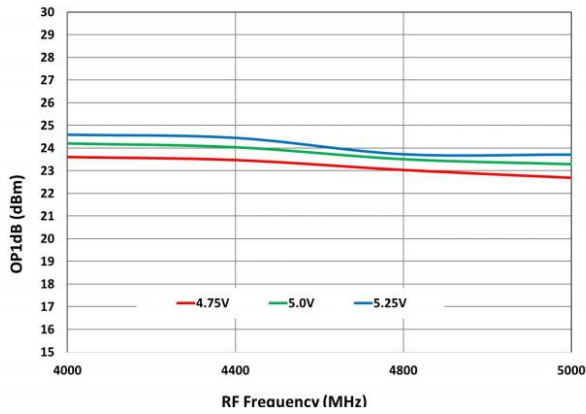


Figure 14. P1dB (High Power Mode) Vs. Temp – 5V

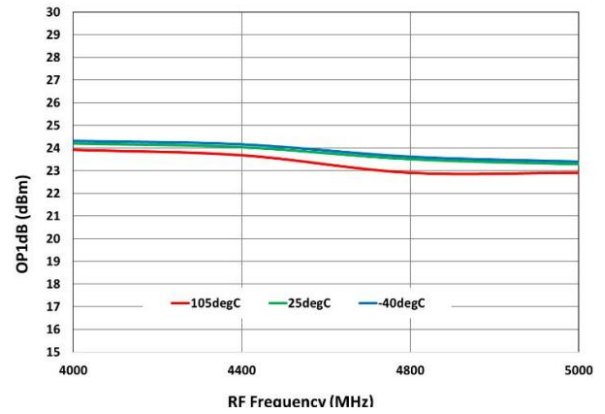


Figure 15 P1dB (Low Power Mode) Vs. Volt– 25 °C

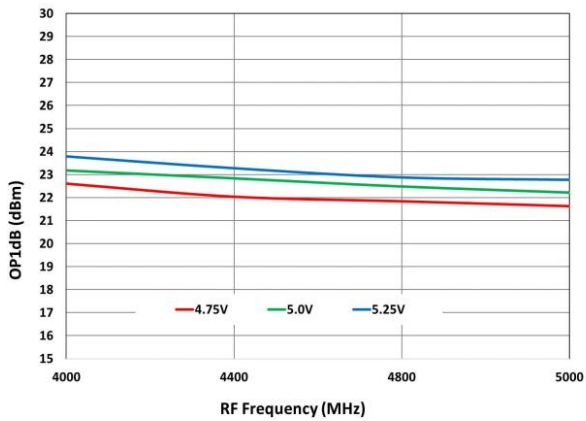
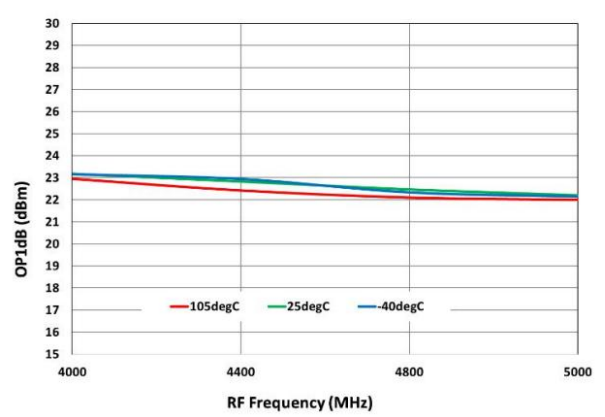


Figure 16 P1dB (Low Power Mode) Vs. Temp – 5V



P1dB

Test conditions unless otherwise noted: 25 °C, VDD = STBY = +5Vdc test on HOTLO Application Board

Figure 17 Noise Figure vs. Temp – 5V

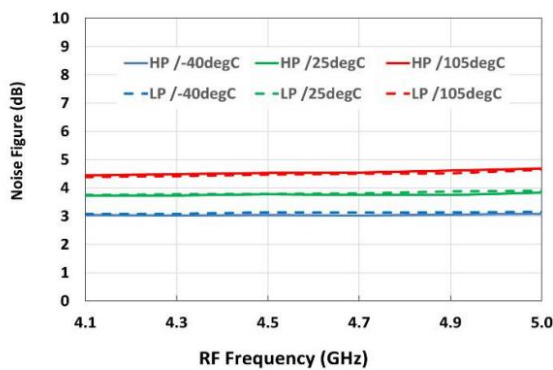
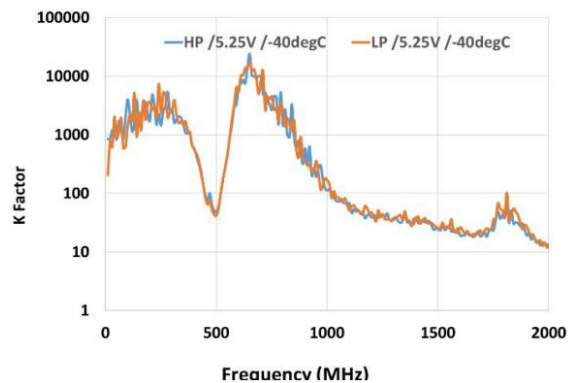


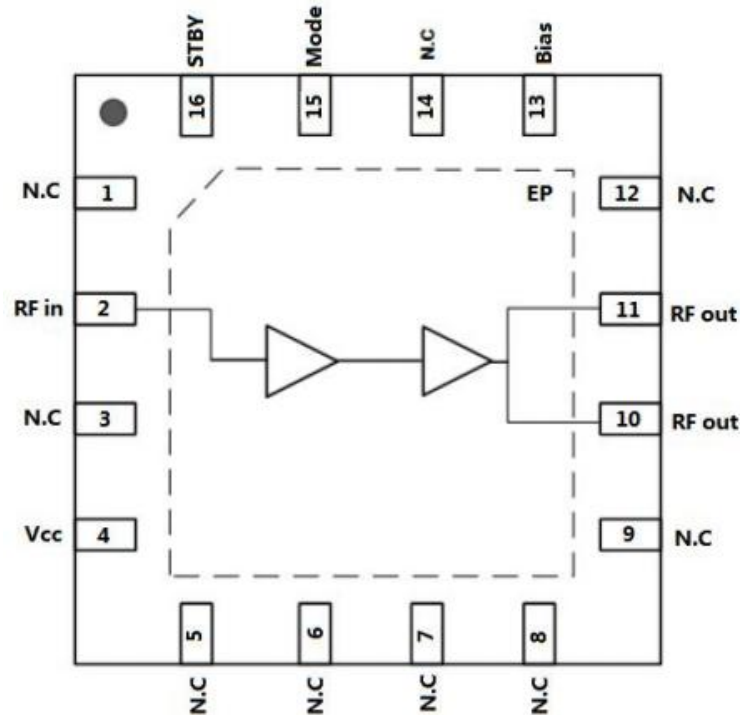
Figure 18. K Factors (Low Band)



NF & K-Factor

Test conditions unless otherwise noted: 25 °C, VDD = STBY = +5Vdc test on HOTLO Application Board

Pin Configuration and Description



Reference	Value	Description
1, 3, 5, 6, 7, 8, 9, 12, 14	NC	Not Connected
2	RF IN	RF Input
4	VCC	Voltage Supply
10	RF OUT	RF Output
11	RF OUT	RF Output
13	BIAS	Voltage Biasing
15	MODE	High Power mode/Low Power mode selection: Refer to R2 in BOM
16	STBY	Chip Enable: Low level --> OFF High level --> ON
EP	GND	Ground

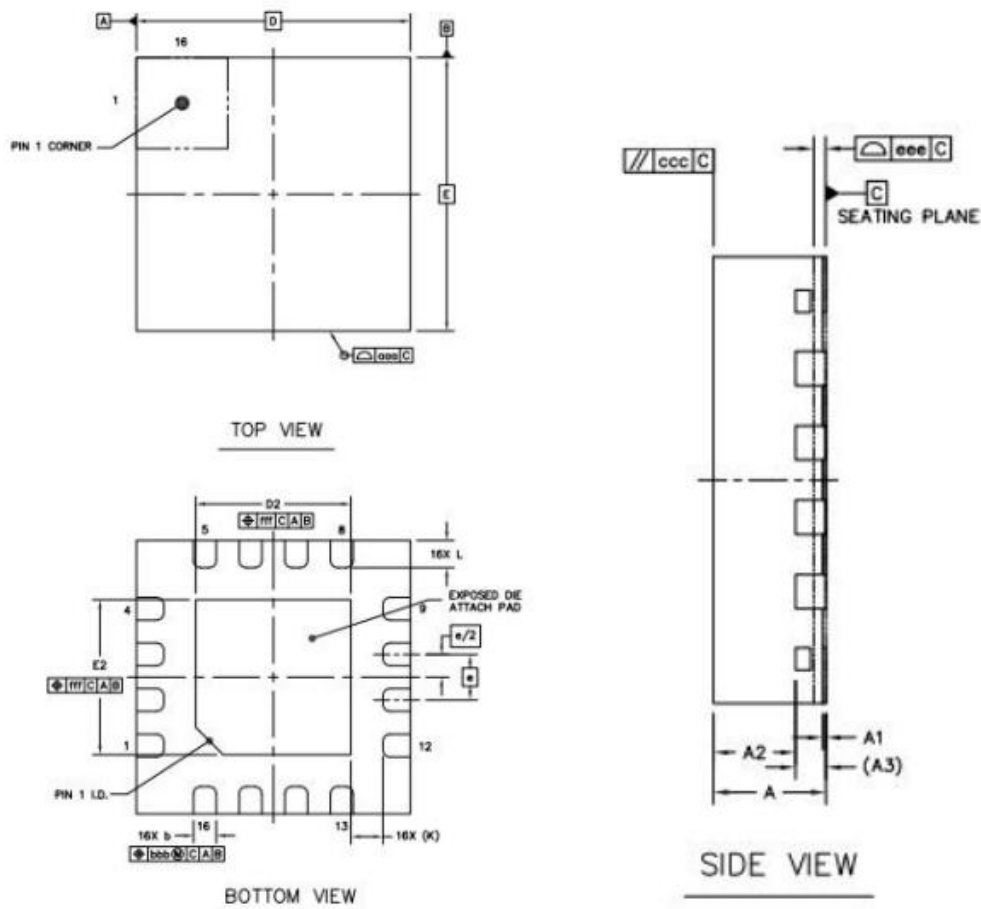
Package Marking and Dimensions



- Line1 (fixed): Device name in W/O
- Line2 (unfixed): Marking Lot No in W/O (Sample: E596-20140001)
- Line3 (unfixed): Date Code + JY

This Marking SPEC only stipulates the content of Marking. For marking requirements such as font and size, please refer to the latest version of "Holto Product Printing Specification"

Marking




ITEM	Symbol	MIN	TYP	MAX
Total Thickness	A	0.7	0.75	0.8
Stand Off	A1	0	0.02	0.05
Mold Thickness	A2		0.55	
L/F Thickness	A3		0.203	
Lead Width	b	0.2	0.25	0.3
Lead Length	L	0.2	0.3	0.5
Lead Pitch	E		0.5	
Lead-PAD Gap	K		0.35	
Body Size X	D		3	
Body Size Y	E		3	
EP Size X	D2	1.6	1.7	1.8
EP Size Y	E2	1.6	1.7	1.8
Size Offset	fff		0.1	
Coplanarity	eee		0.08	

Package Dimensions

Tape and Reel Information

Handling Precautions

Parameter	Grade
Moisture Sensitivity Level MSL	3

Parameter	Rating	Standard	
ESD – Human Body Model (HBM)	Class 1B	JESD22-A114	
ESD – Human Body Model (MM)	Class A	EIA/JESD22-A115	
ESD – Charged Device Model (CDM)	Class III	JESD22-C101	

RoHS Compliance

This product is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU.

Datasheet Status

Document status	Product status	Definition
Objective Datasheet	Design simulation	Product objective specification
Preliminary Datasheet	Customer sample	Engineering samples and first test results
Product Datasheet	Mass production	Final product specification

Abbreviations

Acronym	Definition
LD MOS	Laterally-Diffused Metal-Oxide Semiconductor
CW	Continuous Waveform

Revision history

Document ID	Datasheet Status	Release Date	Revision Version
Rev 2.1	Product	Marcg2021	Update upper and lower limit specifications
Rev 2.2	Product	March 2023	New format based on English version datasheet
Rev 2.3	Product	April 2024	Update package marking information

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations and information about HOLTLO:

- Web: www.andesource.com
- Email: andehk@andesource.com

For technical questions and application information:

- Email: andetech@andesource.com

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