H8G3336M12P

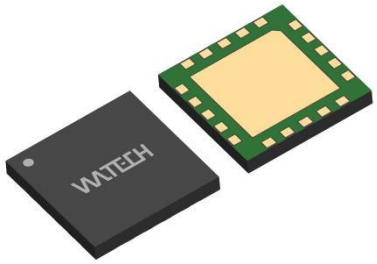
12.5W, 3.3 - 3.6 GHz LDMOS MMIC Amplifier

Product datasheet

Description

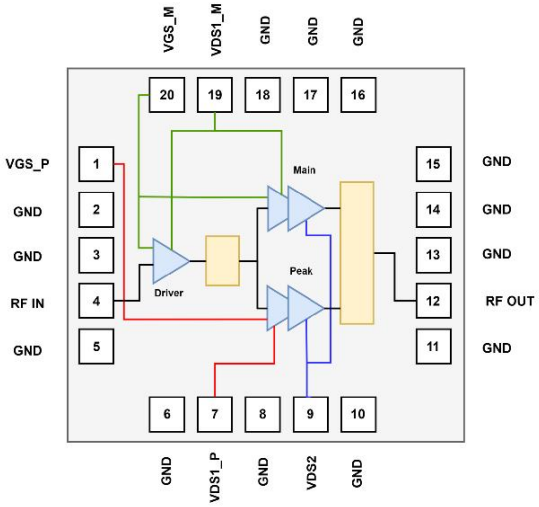
The H8G3336M12P is a LDMOS MMIC Integrated Asymmetrical Doherty based on 3-Stage with 12.5W saturated output power covering frequency range from 3.3 to 3.6 GHz.

The amplifier is 50 Ω Input/Output matched with a small compact footprint 7x7 mm which makes it ideal for integration.



20 Pin LGA 7x7 mm Plastic Package

Block Diagram



H8G3336M12P Block Diagram

Features

- Operating Frequency Range: 3.3 to 3.6 GHz
- Operating Drain Voltage: +28V
- Saturation Output Power: 12.5W
- 50 Ω Input/Output matched
- Integrated Input Divider
- Integrated Output Combiner
- Integrated Asymmetrical Doherty Final Stage
- High Efficiency: 33.6%@3.45GHz, WCDMA
- High Gain: 34.6dB@3.45 GHz, WCDMA
- Small footprint package: LGA 7x7 mm

Applications

- 3GPP 5G NR FR1 n77/78 and 4G-LTE band B42/43
- Power Amplifier for Small Cells
- Driver Amplifier for Micro and Macro Base Stations
- Active Antenna Array for 5G mMIMO
- Repeaters/DAS
- Mobile Infrastructure

Ordering Information

Part Number	Description
H8G3336M12P	Reel Package
H8G3336M12PEVB	3.3 to 3.6 GHz EVB

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Typical Performance

RF Characteristics (Pulsed CW)

Freq (GHz)	P3dB (dBm)	Gain (dB)	Eff (%)	IRL (dB)
3.3	41.7	34.0	35.9	12.0
3.45	41.7	35.0	35.2	13.1
3.6	41.3	34.6	33.1	11.7

Test conditions unless otherwise noted: 25 °C, V_{DD} = +28Vdc, I_{DQ} = 45 mA, Vgsp = Vgsm-0.5V, Pulse Width = 100 us, Duty Cycle = 10% test on HOTLO Application Board

RF Characteristics (WCDMA)

Freq (GHz)	Gain (dB)	Eff (%)	IRL (dB)	ACPR* @5MHz (dBc)	ACPR* @10MHz (dBc)
3.3	33.7	32.6	12.0	-30.5	-41.0.
3.45	34.6	33.6	12.9	-29.7	-41.2
3.6	33.8	32.4	11.3	-29.3	-41.1

Test conditions unless otherwise noted: 25 °C, V_{DD}=+28Vdc, I_{DQ} = 45 mA, Vgsp = Vgsm-0.5V, P_{AVG} = 32 dBm
1C-WCDMA 5MHz Signal, 7.6 dB PAR @ 0.01% CCDF test on HOTLO Application Board
**Uncorrected DPD*

Absolute Maximum Ratings

Parameter	Range/Value	Unit
Drain voltage (V_{DSS})	-0.5 to +65	V
Gate voltage (V_{GS})	-5 to +10	V
Drain voltage (V_{DD})	0 to +28	V
Storage Temperature (T_{STG})	-55 to +150	°C
Case Temperature (T_C)	-40 to +125	°C
Junction Temperature (T_J)	-40 to +175	°C

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Electrical Specification

DC Characteristics

Parameter	Conditions	Min	Typ	Max	Unit
Breakdown Voltage $V_{(BR)DSS}$	Vgs=0V, Ids=100uA	65	-	-	V
Gate-Source Threshold Voltage $V_{GS(th)}$	Vgs=Vds, Ids=5.2uA	1.2	-	1.8	V
Drain Leakage Current I_{DSS}	Vgs=0V, Vds=28V	-	-	0.5	uA
Gate Leakage Current I_{GSS}	Vgs=5V, Vds=0V	-	-	0.05	uA

RF Characteristics (Pulsed CW)

Parameter	Freq (GHz)	Min	Typ.	Max	Unit
P3dB	3.6	41.0	41.5	-	dBm

Test conditions unless otherwise noted: 25 °C, V_{DD} = +28Vdc, I_{DQ} = 45 mA, Vgsp = Vgsm-0.5V, Pulse Width = 100 us, Duty Cycle = 10% test on HOTLO Production Board

RF Characteristics (WCDMA)

Parameter	Conditions	Min	Typ.	Max	Unit
Frequency	3.6				GHz
Gain	P_{AVG} = 32 dBm	30.5	33.5	35	dB
Eff	P_{AVG} = 32 dBm	28	31	-	%
IRL	P_{AVG} = 32 dBm	10	13	-	dB
ACPR@5MHz (Uncorrected)	P_{AVG} = 32 dBm	-	-30	-26	dBc

Test conditions unless otherwise noted: 25 °C, V_{DD}=+28Vdc, I_{DQ} = 45 mA, Vgsp = Vgsm-0.5V, 1C-WCDMA 5MHz Signal, 7.6 dB PAR @ 0.01% CCDF test on HOTLO Production Board

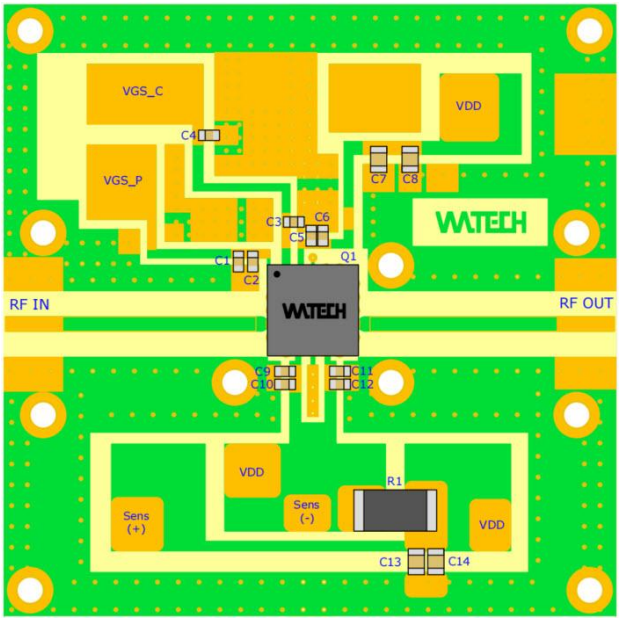
Load Mismatch Test

Condition	Test Result
VSWR=10:1, at all Phase Angles, V_{DD}=+28Vdc, I_{DQ} = 45 mA, Vgsp=Vgsm-0.5V, 1C-WCDMA 5MHz Signal, 7.6 dB PAR @ 0.01% CCDF, Frequency tested 3.3, 3.45 and 3.6 GHz P_{AVG} = 35 dBm test on HOTLO Application Board	No Device Degradation

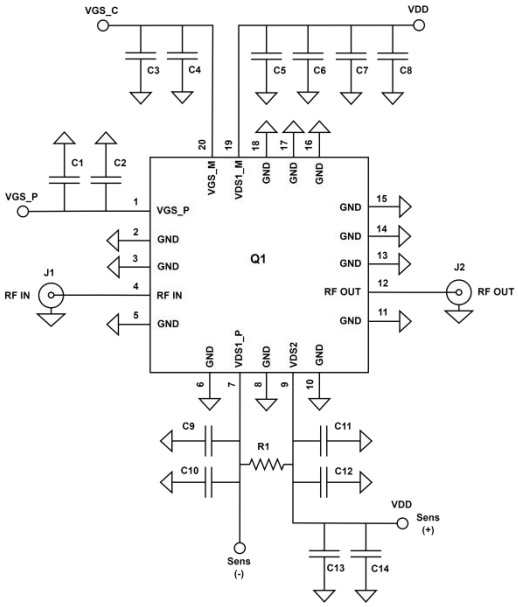
Thermal Information

Parameter	Condition	Value (Typ)	Unit
Thermal Resistance Junction to Case (R_{TH})	T_{CASE}= 90°C, 1C-WCDMA 5MHz Signal, 7.6 dB PAR, P_{AVG} = 32 dBm	9.8	°C /W

H8G3336M12P 3.3 – 3.6 GHz Reference Design (47 x47 mm)



EVB Layout

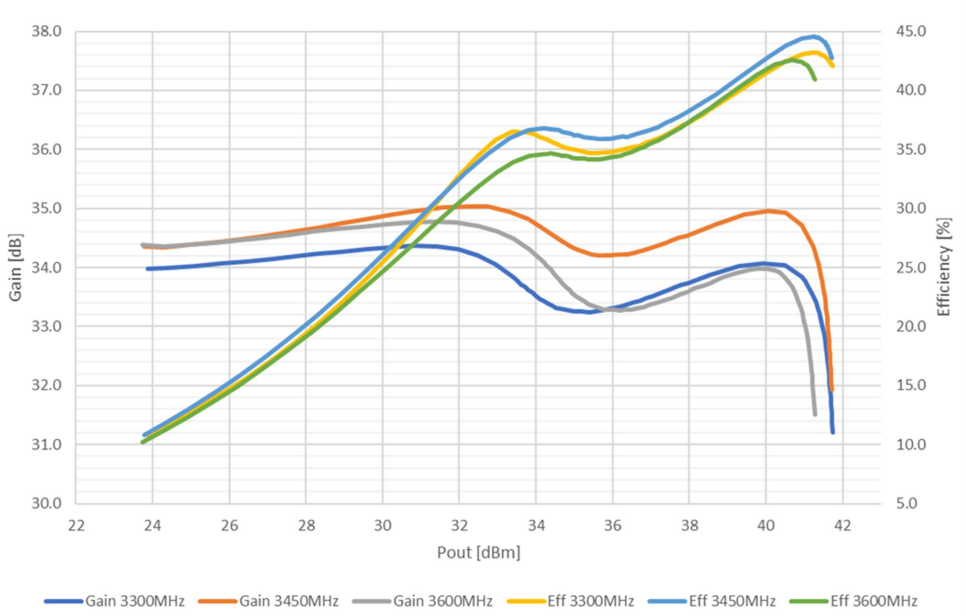


EVB Schematic

Bill of Materials (BoM) - H8G3336M12P 3.3 – 3.6 GHz Reference Design

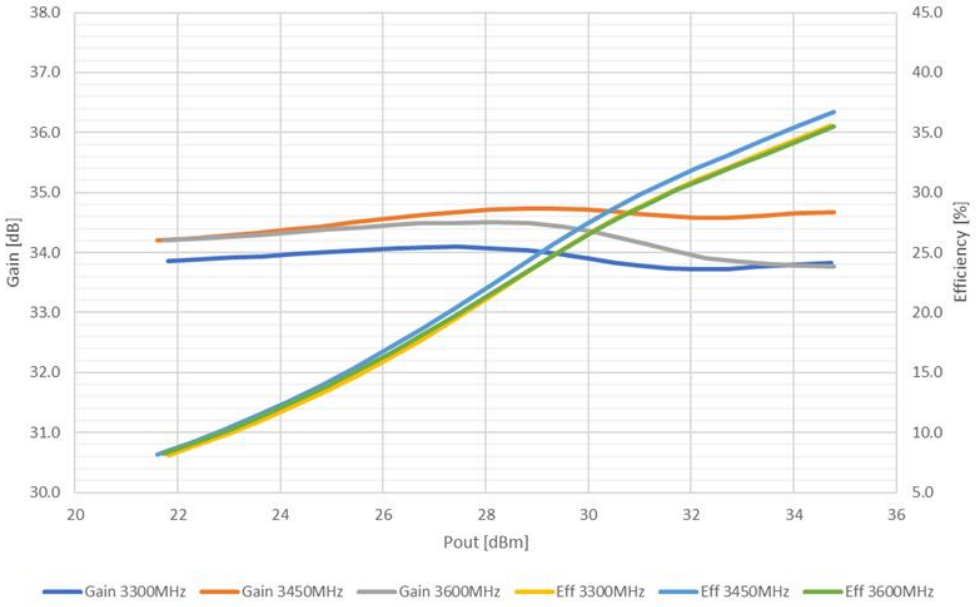
Reference	Value	Description	Manufacturer	P/N
Q1	-	12.5W, 3.3 - 3.6 GHz LDMOS MMIC PA	Holto	H8G3336M12P
C7,C8, C13,C14	1uF ±10%, 0805	Multi-Layer Ceramic Capacitor	Murata	GRM219R7YA105KA12
C1-C6, C9 - C12	1uF ±10%, 0603	Multi-Layer Ceramic Capacitor	Murata	GCM188R71E105KA64D
R1	100mΩ/1W, 0.1%	High-Precision Resistor	Vishay	Y44870R10000B0R
PCB	• Rogers 4350B, er = 3.66; Thickness= 20 mil (0.508 mm); Thickness copper plating = 35 µm (1oz) • Soldered on a 47x47x10 mm Copper Base-Plate			

Performance Plots



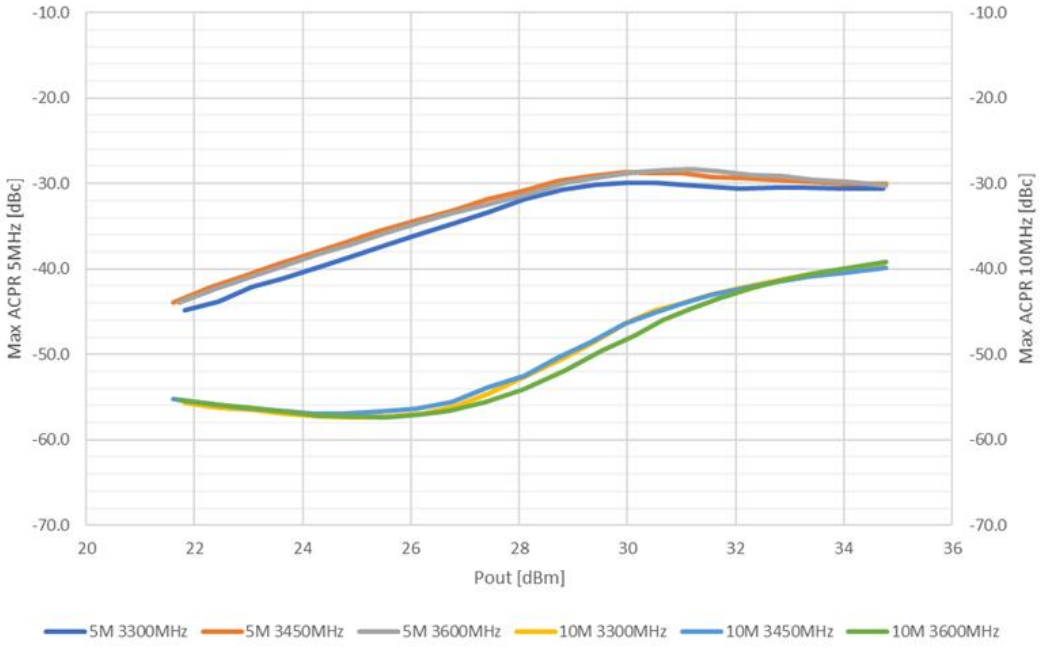
Pulsed CW, Gain and Efficiency vs Pout

Test conditions unless otherwise noted: 25 °C, V_{DD} = +28Vdc, I_{DQ} = 45 mA, Vgsp = Vgsm-0.5V, Pulse Width = 100 us, Duty Cycle = 10% test on HOTLO Application Board



WCDMA, Gain and Efficiency vs Pout

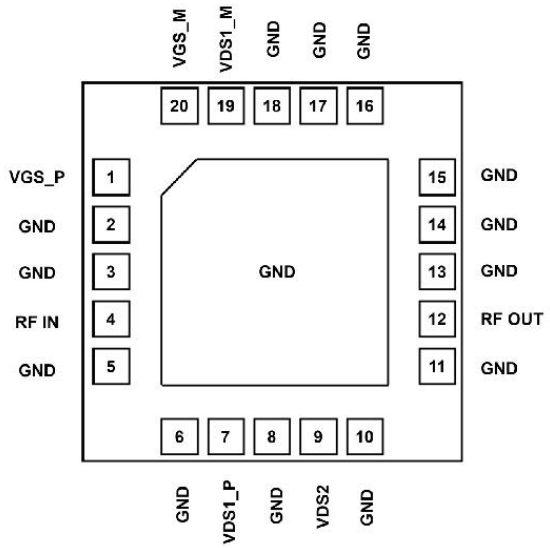
Test conditions unless otherwise noted: 25 °C, V_{DD}=+28Vdc, I_{DQ} = 45 mA, Vgsp = Vgsm-0.5V, 1C-WCDMA 5MHz Signal, 7.6 dB PAR @ 0.01% CCDF test on HOTLO Application Board



WCDMA, ACPR 5MHz and 10MHz vs Pout

Test conditions unless otherwise noted: 25 °C, V_{DD}=+28Vdc, I_{DQ} = 45 mA, Vgsp = Vgsm-0.5V, 1C-WCDMA 5MHz Signal, 7.6 dB PAR @ 0.01% CCDF test on HOTLO Application Board

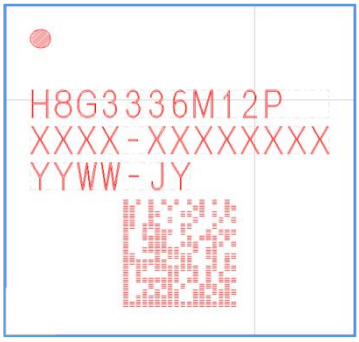
Pin Configuration and Description



Pinout Device Configuration

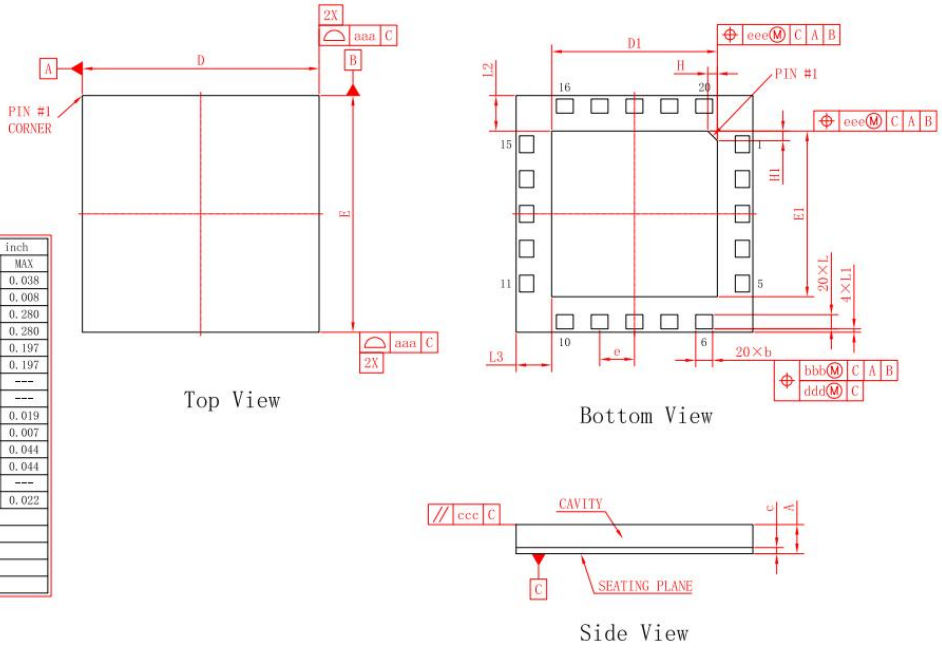
Pin Number	Label	Description
1	VGS_P	Gate-Source Voltage Peak
2	GND	Ground
3	GND	Ground
4	RFIN	RF Input
5	GND	Ground
6	GND	Ground
7	VDS1_P	Drain-Source Voltage Peak Driver
8	GND	Ground
9	VDS2	Drain-Source Voltage Final Stage
10	GND	Ground
11	GND	Ground
12	RFOUT	RF Output
13	GND	Ground
14	GND	Ground
15	GND	Ground
16	GND	Ground
17	GND	Ground
18	GND	Ground
19	VDS1_M	Drain-Source Voltage Main Driver
20	VGS_M	Gate-Source Voltage Main

Package Marking and Dimensions



- LIne1 (fixed): Device name in W/O
- Line2 (unfixed): Marking Lot No in W/O (Sample: E596-20140001)
- Line3 (unfixed): Date Code + JY
- This Marking SPEC only stipulates the content of Marking. For marking requirements such as font and size, please refer to the latest version of "Holto Product Printing Specification"

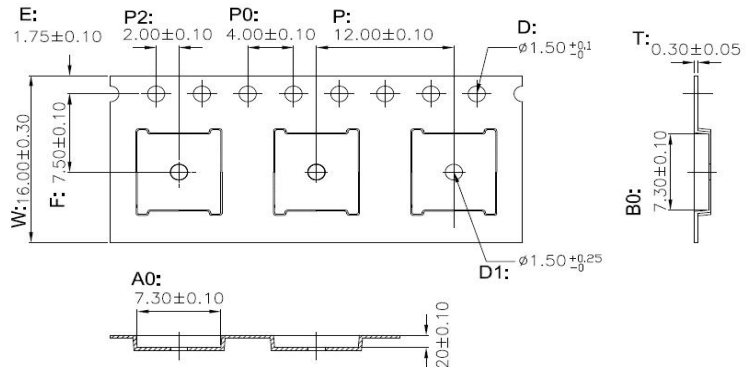
Marking



symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.760	0.860	0.960	0.030	0.034	0.038
c	0.150	0.180	0.210	0.006	0.007	0.008
D	6.900	7.000	7.100	0.272	0.276	0.280
E	6.900	7.000	7.100	0.272	0.276	0.280
D1	4.800	4.900	5.000	0.189	0.193	0.197
E1	4.800	4.900	5.000	0.189	0.193	0.197
H	---	0.286	---	---	0.011	---
H1	---	0.286	---	---	0.011	---
L	0.370	0.420	0.470	0.015	0.017	0.019
L1	0.025	0.100	0.175	0.001	0.004	0.007
L2	0.975	1.050	1.125	0.038	0.041	0.044
L3	0.975	1.050	1.125	0.038	0.041	0.044
e	---	1.030	---	---	0.041	---
b	0.450	0.500	0.550	0.018	0.020	0.022
aaa	0.150			0.006		
bbb	0.150			0.006		
ccc	0.100			0.004		
ddd	0.080			0.003		
eee	0.150			0.006		

Package Dimensions

Tape and Reel Information



Notes:

1. Carrier tape color: BLACK.
2. Carrier material :PS (Polystyrene).
3. ESD surface resistivity < 1× 1011 Ω/square per EJA, JEDEC TNR specification.
4. Heat deflection temperature for Tape & Reel material: 62°C
5. Vicat softening temperature (10N) for Tape & Reel material: 95°C
6. Dimension is millimeter.

Tape & Reel Packaging Descriptions

Tape & Reel Packaging Descriptions

Handling Precautions

Parameter	Grade
Moisture Sensitivity Level MSL	3

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 1B	JESD22-A114
ESD – Human Body Model (MM)	Class A	EIA/JESD22-A115
ESD – Charged Device Model (CDM)	Class III	JESD22-C101

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RoHS Compliance

This product is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU.

Datasheet Status

Document status	Product status	Definition
Objective Datasheet	Design simulation	Product objective specification
Preliminary Datasheet	Customer sample	Engineering samples and first test results
Product Datasheet	Mass production	Final product specification

Abbreviations

Acronym	Definition
LDMOS	Laterally-Diffused Metal-Oxide Semiconductor
CW	Continuous Waveform
VSWR	Voltage Standing Wave Ratio

Revision history

Document ID	Datasheet Status	Release Date	Revision Version
Rev 3.1	Production	2021/08/12	Updated Marking
Rev 3.2	Production	2021/08/20	Update Minimum Gain value of 30.5 dB (Electrical Spec. > RF Characteristics (WCDMA))
Rev 3.3	Production	2021/09/13	Update real picture product on Tape & Reel Packaging Descriptions figure
Rev 3.4	Production	2022/2/25	Update Maximum IDSS and IGSS values (Electrical Spec. > DC Characteristics)
Rev 3.5	Production	2022/4/21	Mark the Main Gate Leakage Current (IDSS) and the Peak Gate Leakage Current separately (Electrical Spec. > DC Characteristics)
Rev 3.6	Production	2023/01/03	New format based on English version datasheet

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Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations and information about HOTLO:

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For technical questions and application information:

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